EXHIBIT 15

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

ARM LTD.,

        Plaintiff,

        v.

QUALCOMM INC., QUALCOMM
TECHNOLOGIES, INC. and NUVIA, INC.,

        Defendants.

C.A. No. 22-1146 (MN)

EXPERT REBUTTAL REPORT OF JOEL H. STECKEL, PH.D.

February 27, 2024

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I.   INTRODUCTION

A. Qualifications

1.   I am a Professor of Marketing at the Leonard N. Stern School of Business, New York University ("NYU Stern"), where I have taught since January 1989. I served as NYU Stern's Vice-Dean for Doctoral Education from August 2012 to September 2021. Overlapping that interval, I also served as the Acting Chairperson of the school's Accounting Department from August 2016 to August 2019. Prior to my promotion to Vice Dean, I was the faculty director of the Stern School Doctoral Program for five years, from May 2007 to July 2012. Earlier I served as the Chairperson of NYU Stern's Marketing Department for six years, from July 1998 to June 2004. I have also held either permanent or visiting faculty appointments at the Graduate School of Business, Columbia University; the Anderson Graduate School of Management, U.C.L.A.; the School of Management, Yale University; and the Wharton School, University of Pennsylvania. This past academic year (2022-2023) I was on sabbatical and served as a Visiting Scholar at the University of Pennsylvania Carey Law School.

2.   I received my B.A. *summa cum laude* from Columbia University in 1977, and M.B.A. (with distinction), M.A., and Ph.D. degrees from the Wharton School, University of Pennsylvania in 1979, 1980, and 1982, respectively. I was elected to *Phi Beta Kappa* at Columbia University and *Beta Gamma Sigma* at the Wharton School. These are the national honor societies for the respective disciplines I studied at these institutions.

3.   I was the Founding President of the INFORMS (Institute for Operations Research and Management Science) Society on Marketing Science ("ISMS"), the foremost professional group for the development and application of management science theory and tools in

marketing. In addition, I am a member of the American Marketing Association, the American Statistical Association, the Association for Consumer Research, the American Psychological Association, the American Association for Public Opinion Research, and the Society for Consumer Psychology.

4. My fields of specialization within marketing include marketing research methodologies such as marketing and branding strategies, the relationship between marketing research and marketing strategy, managerial decision-making, consumer decision-making, and the study of consumer perceptions of trademarks. I am an author or editor of five books and over 60 articles. In the course of my scholarly research, teaching, and consulting work, I have studied issues of marketing research, branding, and their roles in consumer choice and marketing strategy. In particular, I have studied methodologies for assessing consumer perceptions of trademarks.

5. I have sat on the editorial boards of many major journals over the years. From July 2010 until March 2017, I served as a co-Editor-in-Chief of the journal *Marketing Letters*. In that capacity, I evaluated over 200 research studies each year for over six and a half years. I served as a gatekeeper, deciding which articles were published in the journal, and which were not. As such, my evaluations of the scientific reliability and validity of each research study were subject to the scrutiny of the academic community. The community considers any study that appeared in the journal that did not conform to the scientific standards of my profession as a black mark on my record. I consider the fact that the journal's publisher, the international firm, Springer-Verlag, kept me on long past the expiration of my term (July 2014) as validation of my performance in evaluating scientific research. My

professional qualifications are described further in my curriculum vitae, which is attached as **Appendix A**.

6.   During the course of my professional career, I have designed, conducted, supervised, and/or evaluated hundreds of consumer surveys. In that work, I have formulated sampling strategies, designed questionnaires, analyzed data, and interpreted results. I have also evaluated similarly purposed survey work performed by others.

7.   I have served as an expert witness on marketing research, marketing strategy, branding, trademark, and issues related to consumer decision-making in a variety of litigation matters. In the past four years, I testified as an expert witness in the matters listed in **Appendix B**.

8.   My rate of compensation for this assignment is $1,250 per hour. Others at Analysis Group, Inc. ("AG"), an economic and litigation consulting firm headquartered in Boston, Massachusetts, performed part of the work for this assignment under my direction. I receive additional compensation from AG related to the work of others under my supervision. No compensation is contingent upon the outcome of this research or of the case.

B. Case Background

9.   Plaintiff Arm Ltd. ("Arm" or "Plaintiff") "develop[s] processor architectures, including instruction set architectures, and processor core designs implementing those architectures."[1] According to the Complaint, Arm "does not manufacture or sell chips," but rather licenses its chip technology to other companies "to use in developing their own

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[1]   Complaint, *Arm Ltd. v. Qualcomm Inc., Qualcomm Technologies, Inc., and NuVia, Inc.,* Case No.: 1:22-cv-01146-UNA, United States District Court for the District of Delaware, August 31, 2022 ("Complaint"), ¶ 11.

chips or in their own electronic devices."[2] Arm "monetize[s] its research and intellectual property by receiving both licensing fees and royalties for products incorporating Arm's technology and intellectual property."[3] I understand from the Complaint that, according to Arm, "there are two main types of Arm licenses for Arm's technologies: Technology License Agreements ('TLAs'), which allow the use of specific 'off-the-shelf' Arm processor core designs with only minor modifications, and Architecture License Agreements ('ALAs'), which allow for the design of custom processor cores that are based on particular architectures provided by Arm."[4] I understand that Arm-built cores are licensed under TLAs and Qualcomm custom cores are licensed under ALAs.

10.   Defendants are Qualcomm, Inc. and Qualcomm Technologies, Inc. (collectively, "Qualcomm") and NuVia, Inc. ("Nuvia"), together "Defendants." According to the Complaint, "Qualcomm is one of the world's largest semiconductor companies, with a portfolio of intellectual property and products directed to wireless technologies, including cellular, Bluetooth, and Wi-Fi; CPUs and ICs; networking; mobile computers; cell phones; wearables; cameras; automobiles; and other electronic devices."[5] Nuvia was a startup founded in 2019 that "planned to design energy-efficient CPUs for data center servers based on a custom processor implementing the Arm architecture."[6]

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[2]   Complaint, ¶ 14.

[3]   Complaint, ¶ 16.

[4]   Complaint, ¶ 17.

[5]   Complaint, ¶ 25.

[6]   Complaint, ¶ 20.

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11.   I understand that Arm granted Nuvia both an ALA and TLA in 2019,[7] and through 2021

Nuvia designed custom processor cores.[8] █████████████████████████████

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12.   I further understand that Qualcomm also has an Arm ALA and TLA.[12] ███████████

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[7]   Complaint, ¶ 21.

[8]   Complaint, ¶ 23.

[9]   QCARM_0337839–855 at 843.

[10]   ARM_00111099–113 at 103.

[11]   QCARM_0337839–855 at 843; ARM_00111099–113 at 103.

[12]   Complaint, ¶¶ 26-27.

[13]   ARM_00055357–399 at 363.

[14]   ARM_00060458–512 at 462. █████████████████████████████████

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[15]   ARM_00055357–399 at 363; ARM_00060458–512 at 462.

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13.   Qualcomm announced on January 13, 2021 that it was acquiring Nuvia,[16] and ultimately

completed the acquisition in March 2021.[17] According to the Defendants' Amended

Answer to Plaintiff's Complaint, after the Nuvia acquisition, under its own agreements with

Arm, Qualcomm continued work that Nuvia had started on its custom core and a "system

on a chip" (SoC) for the server market.[18] I understand from the Defendants' Amended

Answer that Qualcomm's work on that technology carried on for about a year without

disruption.[19] Plaintiff asserts that, in a January 2022 press release, Qualcomm "tout[ed] the

'broad support from ecosystem partners for the PC industry's transition to Arm®-based

computing,' with Qualcomm's CEO confirming that '[t]he future of the PC industry is

modern Arm-based architectures.'"[20]

14.   According to the Complaint, Arm terminated both Nuvia licenses effective March 1, 2022,

and reminded Qualcomm and Nuvia "of their obligations upon termination to stop using

and destroy the Nuvia technology developed under the now-terminated licenses."[21] I

understand that Qualcomm disputes that it was obligated to stop using and destroy any

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[16]   Complaint, ¶ 28.

[17]   "Qualcomm Completes Acquisition of Nuvia," *Qualcomm*, March 15, 2021, available at
       https://www.qualcomm.com/news/releases/2021/03/qualcomm-completes-acquisition-nuvia.

[18]   Defendants' Answer and Defenses to Plaintiff's Complaint and Jury Demand and Defendants' Amended
       Counterclaim, *Arm Ltd. V. Qualcomm Inc., Qualcomm Technologies, Inc. and NuVia, Inc.,* Case No. 22-
       1146 (MN), United States District Court for the District of Delaware, October 26, 2022 ("Defendants'
       Amended Answer"), ¶ 30 ("Meanwhile, throughout 2021 to the present day and with full knowledge by
       ARM, Qualcomm continued development work on the ███████████████████████████████
       ███, as was its right under Qualcomm's own license agreements with ARM.").

[19]   Defendants' Amended Answer, ¶ 240 ("Despite ARM's demand that Qualcomm destroy and stop using
       NUVIA technology, for approximately one year, ARM continued to provide verification support to
       Qualcomm in developing the ████████████ and related SoCs, and also continued to acknowledge the
       Defendants' rights under the Qualcomm ALA and TLA to that technology.").

[20]   Complaint, ¶ 38.

[21]   Complaint, ¶ 39.

technology as a result of this demand, but that it carried out a process to fulfill Arm's request and certified that it had done so. [22]

15.   Plaintiff alleges that after the termination, "based on Qualcomm's public announcements of its plans to use Nuvia technology," Qualcomm "likely […] has continued to retain and use Nuvia technology developed pursuant to the Nuvia licenses, thereby materially breaching the termination provisions of those licenses." [23]

16.   Plaintiff alleges that "[t]he failure of Nuvia and Qualcomm to comply with the post-termination obligations under the Nuvia ALA is causing, and will continue to cause, irreparable harm to Arm." [24] Plaintiff further alleges that "Qualcomm and Nuvia's unauthorized use of the ARM Marks […] is likely to cause confusion, mistake, or deception on the part of consumers as to the affiliation, connection, or associations of Defendants with Arm, or as to the origin, sponsorship, or approval or Defendants' semiconductor chips using the relevant Nuvia technology." [25]

17.   I understand that Qualcomm contends that the ALA "is intended to encourage licensees to develop their own CPU core technology with their own innovations, at their own risk and expense and for their benefit," [26] and that "Qualcomm can, under the ALA, design, manufacture, and distribute Qualcomm's custom ARM-compatible CPU cores." [27]

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[22]   Defendants' Amended Answer, ¶¶ 36-37.

[23]   Complaint, ¶ 52.

[24]   Complaint, ¶ 54.

[25]   Complaint, ¶ 77.

[26]   Defendants' Amended Answer, ¶ 43.

[27]   Defendants' Amended Answer, ¶ 183.

C. The Dhar Report's Opinions

18. Plaintiff retained Dr. Ravi Dhar, Ph.D., "to opine, from a marketing and consumer behavior perspective, on the following issues:

    a. [t]he benefit of a strong mark in the marketplace;

    b. [w]hether Arm's Trademarks and brand are distinctive and strong in the United States marketplace context;

    c. [w]hether Qualcomm's unlicensed use of the Arm Trademarks in connection with 'Nuvia Products' […] would likely result in confusion […]; [and]

    d. [w]hether Qualcomm's use of the Arm Trademarks is likely to cause harm by impacting the brand or result in a loss of sales by Arm and Arm's licensees that serve the same market." [28]

19. To address this assignment, Dr. Dhar states that he "reviewed case specific materials provided to [him] by counsel, as well as other documents" [29] and "drew on [his] knowledge, education, and experience in marketing and branding developed over the past several decades" in forming his opinions. [30] Based on those materials and background, Dr. Dhar concluded that:

    a. "Arm's brand and Trademarks are strong and confer value in the marketplace;"

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[28] Expert Report of Ravi Dhar Regarding Trademark Infringement, *Arm Ltd. v. Qualcomm Inc., Qualcomm Technologies, Inc.*, *and NuVia, Inc.,* C.A. No. 22-1146-MN, United States District Court for the District of Delaware, December 20, 2022 ("Dhar Report"), ¶ 9.a-d.

[29] Dhar Report, ¶ 12.

[30] Dhar Report, ¶ 12.

b.   "Qualcomm's prior history and usage of Arm's Trademarks […] demonstrate a high likelihood that Qualcomm will continue to use Arm's Trademarks in connection with its future products, particularly Nuvia Products;"

c.   "Qualcomm's use of Arm's Trademarks is likely to cause customer confusion;" and

d.   Qualcomm's "unauthorized use is […] likely to cause harm to Arm" via "loss of control to Arm of its brand and goodwill" and "divert[ing] customers away from Arm."[31]

D. Assignment

20.   I was asked by Paul, Weiss, Rifkind, Wharton, & Garrison LLP, Counsel for Qualcomm, to review and assess the Expert Report of Ravi Dhar (the "Dhar Report"). Specifically, I was asked to assess the validity of the conclusions offered in the Dhar Report in light of the evidence Dr. Dhar presented.

21.   In formulating my opinions, I have considered the Dhar Report, materials considered by Dr. Dhar, and the materials cited in the footnotes of this rebuttal report and listed in **Appendix C**. Should additional relevant documents or information be made available to me, I may amend or supplement my opinions as appropriate.

II.   SUMMARY OF CONCLUSIONS

22.   Based on my review of the Dhar Report and other case materials, I conclude the following:

23.   The Dhar Report does not meet the standards for a rigorous scientific analysis under accepted industry practices and academic guidelines. The opinions in the Dhar Report are not based on sufficient facts or data. In particular, the selection of sources in the Dhar

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[31]   Dhar Report, ¶¶ 13-16.

Report appears to be skewed by only considering favorable tidbits in the record, without considering contrary or more holistic evidence. Further, in drawing his conclusions, Dr. Dhar has conducted no research of his own and has not cited any evidence that describes the results of any customer-based research or application. Therefore, the opinions in the Dhar Report amount to little more than subjective personal views about how Dr. Dhar believes the Arm brand may be perceived or whether the use of the Arm Trademarks might cause confusion. Because Dr. Dhar does not apply any replicable methodology beyond his simple say-so to the facts that can be studied, his opinions do not pass scientific muster. See **Section III**.

24. The Dhar Report's assessment of the purported strength of the Arm brand is incomplete and cannot be relied upon.

    a. The Dhar Report fails to provide any customer-based evidence of brand awareness or brand associations. The Dhar Report's evaluation of Arm's brand strength reflects the goals of Arm's branding efforts, but does not examine the extent to which those branding efforts are successful. Such an evaluation would require customer-based evidence. The sources cited in the Dhar Report do not shed light on what actual or potential purchasers of Arm's intellectual property understand the Arm brand to mean. See **Section IV.A**.

    b. The Dhar Report claims that the Arm brand serves as a strong ingredient brand without offering any rigorous assessment. The Dhar Report does not apply to his analysis of Arm's brand any established marketing knowledge or literature about what constitutes a successful ingredient brand. Without any customer-based analysis or application of established marketing knowledge to assess the success of an ingredient brand, the Dhar

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Report cannot establish that the Arm brand is a strong ingredient brand in either Arm's business-to-business ("B2B") market or, ultimately, in end consumers' decisions to purchase an Arm-based end product. See **Section IV.B**.

    c. The Dhar Report fails to take into consideration Qualcomm's own brand and brand strength in its relationship to Arm. The Dhar Report's implication that Arm's brand is an ingredient in the overall success of end products among downstream consumers is unsupported and fails to consider the potentially significant role of other brands and brand components, including Qualcomm's, in these end products' marketing or commercial success. See **Section IV.C**.

25. The Dhar Report's assertion that Qualcomm's use of the Arm Trademarks is likely to cause confusion is baseless.

    a. The Dhar Report inappropriately points to Qualcomm's historical uses of the Arm Trademarks to assume that Qualcomm will likely use the Arm Trademarks in the same way in the future. In particular, the Dhar Report's conclusion that Qualcomm's use of the Arm Trademarks is likely to create confusion is based on the Dhar Report's analysis of Qualcomm's prior use of the Arm Trademarks in connection with Arm-built central processing unit ("CPU") cores, rather than Qualcomm's custom-designed cores that are compatible with the Arm instruction set architecture (the "Arm ISA"). The Dhar Report ignores that Qualcomm's current uses of the Arm Trademarks are distinguished from the Dhar Report's citations of Qualcomm's historical uses of the Arm Trademarks in that they incorporate a modifier like "-based," "-compliant," or "-compatible" and are used in factually accurate statements about Qualcomm's products — not as a branding description of the product itself. See **Section V.A**.

b. The Dhar Report's conclusions regarding confusion are flawed because the Dhar Report fails to consider the sophistication of the B2B industrial procurement departments that purchase Qualcomm's chips, which are highly trained and may therefore be unlikely to be confused by uses of the Arm Trademarks to describe Qualcomm custom cores' technical attributes. Furthermore, the Dhar Report's failure to conduct an empirical analysis of customer confusion, particularly within the relevant market of purchasers, highlights the lack of concrete support for its conclusions. See **Section V.B**.

c. The Dhar Report's assertion that Qualcomm's purported use of the Arm Trademarks creates a false understanding of the custom cores' affiliation, sponsorship, or certification is also unsupported. The Dhar Report offers no empirical analysis to determine whether use of terms such as "Arm-based" or "Arm-compliant" generally connotes any affiliation, sponsorship, approval, validation, or otherwise certification by Arm. The Dhar Report does not present any scientific research necessary to support its conclusion that Qualcomm's purported use of the Arm Trademarks have led to any consumer confusion. See **Section V.C**.

d. The Dhar Report presents no evidence of any actual confusion caused by Qualcomm's purported use of the Arm Trademarks, and the report overlooks admissions by Arm and testimony from Arm's corporate deponents that indicate that Arm itself has been unaware of any actual confusion. See **Section V.D**.

26. The Dhar Report's conclusions on harm to the Arm brand are speculative and do not explain the mechanism by which harm would occur.

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a. The Dhar Report's conclusion about harm to the Arm brand's image and goodwill is speculative and unsupported. Beyond generic unsupported statements that merely explain the general concept of loss of brand image and goodwill, the Dhar Report does not precisely define or otherwise specify what that harm is and how that harm would occur in this specific context. Moreover, the Dhar Report ignores evidence that suggests the opposite, that the Arm brand has not been and is unlikely to be harmed. See **Section VI.A**.

b. The Dhar Report's claim about purported harm to Arm through diversion of sales is overly simplistic, speculative, and unsupported. The Dhar Report does not provide any concrete description of how, or evidence of whether, customers would develop a "mistaken[] understand[ing]" in the sophisticated B2B market in which Qualcomm and other Arm licensees compete.[32] Further, the Dhar Report also does not describe or provide evidence for whether or how this "mistaken[] understand[ing]" would itself cause sales to be diverted from authorized users of Arm Trademarks. See **Section VI.B**.

c. The Dhar Report offers no evidence for its claim that Nuvia customers would be harmed as a result of Qualcomm's use of Arm Trademarks. The Dhar Report fails to establish that potential purchasers of Nuvia products would be deceived about the nature or benefits of the chips they are purchasing, including whether Arm has a license with Qualcomm. See **Section VI.C**.

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[32] Dhar Report, ¶ 132 ("Customers who might have sought out an Arm product may instead turn to Qualcomm's products because they mistakenly understand, because of Qualcomm's infringing use of Arm Trademarks, that Qualcomm's Nuvia Products are equivalent to Arm technology, or somehow supported by Arm.").

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27.   The Dhar Report's analysis of fair use attempts to substitute trademark knowledge for the
judgment of a court. In addition, the Dhar Report's analysis of fair use is speculative and
incomplete. The Dhar Report consistently overlooks and ignores that Qualcomm uses the
Arm Trademarks in connection with its custom cores *referentially* to describe its products'
technical attributes. The Dhar Report does not offer any evidence that Qualcomm's
descriptions of the custom cores as "Arm-based," "Arm-compliant," or "Arm-compatible"
are factually inaccurate, nor does it offer any evidence that relevant customers would take
away an inaccurate understanding of the relationship between Qualcomm and Arm from
those terms. The Dhar Report fails to consider whether Qualcomm's descriptions of its
custom cores as "Arm-based," "Arm-compliant," or "Arm-compatible" are necessary to
accurately identify the custom cores' technical attributes, whether it uses the Arm mark
only to the degree necessary to do that, and that it describes that the custom cores are
compatible with the Arm ISA, which I understand to be accurate. See **Section VII**.

28.   I reserve the right to amend or supplement my opinions, if appropriate, based on additional
information I may receive in the future or additional opinions that Arm's experts may
present.

III.   THE DHAR REPORT DOES NOT MEET THE STANDARDS FOR A RIGOROUS SCIENTIFIC ANALYSIS UNDER ACCEPTED INDUSTRY PRACTICES

29.   It is well-established in the field of marketing research that research must be supported with
objective facts and a scientific research process, which is a "systematic, controlled,

empirical, amoral, public, and critical investigation of natural phenomena."[33] Reasoning without controlled observation and measurement does not constitute science; rather, if a scientist has a hypothesis, it must be tested with an approach that presents "careful logic, organized observation, and measurement that is open to independent scrutiny by others."[34] Thus, one of the cornerstones of scientific research, including marketing research pertaining to branding, is the replicability of a methodology such that the final opinion could be put to an independent test.

30.   As a rebuttal expert, I should be able to investigate and reproduce every step of the analysis an expert performed to derive the conclusions they have reached and the opinions they have put forward. In this case, I should be able to completely examine the way in which the Dhar Report reached its conclusions.

31.   However, the Dhar Report has neither applied nor described any replicable analysis or methods from which it draws the conclusions in the report. Even when only considering the documents Dr. Dhar reviewed, based on the information presented in the Dhar Report, it is not clear how he selected the documents he reviewed, the process by which he reviewed them, and how precisely these reviews informed his conclusions. Further, the Dhar Report states that, in reaching its conclusions, Dr. Dhar leveraged his "knowledge and experience, well-established principles of branding, [his] analysis of documents and testimony provided to [him] by counsel and cited herein, and [his] own independent research."[35]

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[33]   Kerlinger, F.N., and H.B. Lee, *Foundations of Behavioral Research,* Fourth Edition, Cengage Learning, 2000, at p. 14.

[34]   Rosnow, Ralph L. and Robert Rosenthal, *Beginning Behavioral Research*, Seventh Edition, Pearson, 2012, p. 17.

[35]   Dhar Report, ¶¶ 12-13.

However, the Dhar Report does not provide any way to understand how Dr. Dhar applied that knowledge and experience to the relevant facts; nor does it describe what that "independent research" entailed and how it was conducted. Overall, based on my review of the Dhar Report, none of the opinions presented are supported by the results of a replicable scientific process. I discuss three specific flaws below.

32.   *First*, the opinions in the Dhar Report are not based on sufficient facts or data. In particular, the selection of sources in the Dhar Report appears to be skewed by only considering favorable evidence in the record (e.g., testimony by Arm's own representatives) without considering contrary evidence, even from the same documents.[36] I discuss such instances throughout the report. Some examples include the following:

a.   The Dhar Report states that Arm's customers "develop and innovate with Arm's support" and that Arm invests significant efforts in the "design and verification" of its customers processors.[37] This statement, however, relies solely on Arm's 2023 424(b)(4) SEC filing and is belied by — among other things — an article the Dhar Report cites in the very next paragraph.[38]

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[36]   *See* Meyer, M.A., and J.M. Booker, *Eliciting and Analyzing Expert Judgment: A Practical Guide*, SIAM & ASA, 2001, Chapter 3.

[37]   Dhar Report, ¶ 40, citing Arm SEC Form 424(b)(4), September 13, 2023, available at https://www.sec.gov/Archives/edgar/data/1973239/000119312523235320/d550931d424b4.htm#rom55093 1_7.

[38]   *See* Dhar Report, FN 30, citing Shimpi, Anand L., "The ARM Diaries, Part 1: How ARM's Business Model Works," *AnandTech*, June 28, 2013, available at https://www.anandtech.com/show/7112/the-arm-diaries-part-1-how-arms-business-model-works ("Here [under an ALA] you basically get a book and a bunch of tests to verify compliance with the ARM ISA you're implementing. ARM will offer some support to help you with your design, but it's ultimately up to you to design, implement and validate your own microprocessor design.").

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b. The Dhar Report relies on a deposition quote from Jonathan Armstrong, Arm's Head of Brand and Creative Services, to state that third parties are required to contact "Arm's Trademarks team every time it would like to use Arm's word trademarks in connection with a reference to Arm's products, services, or related technologies."[39] This statement, however, is patently incorrect: Arm's Trademark Use Guidelines authorize use of Arm's word marks without prior approval or licensing so long as the use is "accurate, fair and not misleading."[40]

c. The Dhar Report's claim that "Arm's innovation is responsive to consumer demands" is sourced from Arm's 2023 SEC F-1 filing and public statements from Will Abbey, Arm's Chief Commercial Officer, published in *TechCrunch*.[41] Additionally, Arm's December 2021 submission to U.K. regulators at the Competition and Markets Authority shows that the company believed that it was *not* well-positioned to meet these demands.[42]

d. Similarly, the only outside evidence in the Dhar Report's section that supports his conclusions that there has been harm to Arm is deposition testimony again from Mr.

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[39]   Dhar Report, ¶ 56, citing Deposition of Jonathan Armstrong, *Arm Ltd. v. Qualcomm Inc., Qualcomm Technologies, Inc.*, *and NuVia, Inc.*, C.A. No. 22-1146, United States District Court for the District of Delaware, December 8, 2023 ("Armstrong Deposition"), p. 126:11-20.

[40]   QCARM_7517739–744 at 739 ("You may use Arm's trademarks, product names, service names, technology names and other names in text to refer to Arm's products, services and related technology if you follow these guidelines and your use is accurate, fair, and not misleading.").

[41]   Dhar Report, ¶ 104, citing ARM_01259705–0105 at 9715 and Lardinois, Frederic, "Arm After the IPO," *TechCrunch*, September 14, 2023, available at https://techcrunch.com/2023/09/14/arm-after-the-ipo.

[42]   ARM_00088656–684 at 658 ("In addition, Arm does not have the systems building expertise, the software engineering scale, or the R&D resources of x86 vendors like Intel and AMD. Even under the most optimistic projections, standalone Arm could not generate the revenue necessary to invest and compete toe-to-toe with the entrenched x86 incumbents.").

Abbey.[43] Dr. Dhar fails to consider evidence that Arm has *not* been harmed, including in testimony to that effect from Jonathan Armstrong, Arm's Head of Brand and Creative Services,[44] and from Mr. Abbey himself,[45] in addition to evidence of Arm's ample financial success despite Qualcomm's allegedly harmful use of Arm's trademarks.[46]

33.   The Dhar Report's reliance on this evidence, without considering or evaluating contrary evidence that might undermine these statements, makes its assessment of sources highly one-sided.

34.   *Second*, the Dhar Report does not set out any methodology that underpins the basis of his opinions, therefore rendering Dr. Dhar's opinions not scientifically reliable. As noted

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[43]   *See* Dhar Report, Section VIII.D; Dhar Report, ¶¶ 129-130.

[44]   Armstrong Deposition, p. 118:11-23 ("   ").

[45]   *See* Deposition of Will Abbey, *Arm Ltd. v. Qualcomm Inc., Qualcomm Technologies, Inc., and NuVia, Inc.*, C.A. No. 22-1146 (MN), United States District Court for the District of Delaware, October 27, 2023 ("Abbey Deposition").

[46]   *See* "FYE24-Q3 Shareholder Letter," *Arm Holdings plc*, February 7, 2024, available at https://investors.arm.com/static-files/4404a89a-d033-419e-aa0f-d7b15d40e11f, p. 2 ("We had an outstanding Q3 delivering record revenues… Growth was driven by both royalty revenue and license revenue."); Motley Fool Transcribing, "Arm Holdings (ARM) Q3 2024 Earnings Call Transcript," *The Motley Fool*, February 7, 2024, available at https://www.fool.com/earnings/call-transcripts/2024/02/07/arm-holdings-arm-q3-2024-earnings-call-transcript/ ("Record revenues, we exceeded the high end of the range for the guidance and extremely pleased about results overall… Additionally, we are expecting another strong quarter for licensing with revenue up sequentially to near record levels."). "FYE24-Q2 Shareholder Letter," *Arm Holdings plc*, November 8, 2023, available at https://investors.arm.com/static-files/bf24c7a3-d2c0-47bd-bf72-73f686a5d62f, p. 2 ("The better than expected revenue was driven by multiple high-value long-term license agreements signed with industry leading technology companies, and royalty revenue benefiting from market share gains and higher royalty rates."). Further, on an annual basis, Arm's licensing revenue and profits have increased since Qualcomm acquired Nuvia in March 2021. "FYE24-Q2_ArmHoldingsPlc_Historical_Quarters_Datasheet.xlsx," *Arm Holdings plc*, available at https://investors.arm.com/static-files/4de417b7-2ea6-4f60-a1ce-13477d3b28b3, accessed on February 20, 2024.

above, the Dhar Report states that Dr. Dhar conducted "independent research," but does

not describe the basis for that research, its purpose, its methodology, or even its results.

35.　For the kinds of opinions presented in the Dhar Report, I would have expected Dr. Dhar

(or his team) to conduct or otherwise rely upon customer-based evidence and research, for

which many research methods are well-established in the academic literature. For example,

an introductory textbook on strategic brand management describes many qualitative

research techniques (e.g., free association, adjective ratings, personification exercises) and

quantitative techniques (e.g., direct and indirect measures of brand recognition, aided and

unaided measures of brand recall, scale measures of brand attributes and benefits) to assess

potential brand associations and the depth of customers' brand awareness.[47] To assess the

value of brands or ingredient brands, the marketing literature describes numerous methods

to assess brand equity, brand loyalty, brand trust, brand awareness, recognized quality, and

brand associations.[48] To measure the success of an ingredient brand in B2B transactions,

academic literature suggests the use of a "financially oriented measurement tool based on

price premiums" such as conjoint analysis as an input.[49] In drawing his conclusions, Dr.

Dhar has conducted no such research of his own and has not cited any evidence that

describes the results of such customer-based research or applications.

36.　*Third*, as Dr. Dhar has not applied any rigorous methodology to how his facts were selected

or any empirical customer-based analysis to reach his opinions, the opinions in the Dhar

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[47]　*See* Keller, Kevin L., and Vanitha Swaminathan, *Strategic Brand Management: Building, Measuring, and Managing Brand Equity*, Fifth Edition, Pearson, 2020 ("Keller and Swaminathan (2020)"), pp. 332-366.

[48]　*See* Kotler, Philip, and Waldemar Pfoertsch, *Ingredient Branding: Making the Invisible Visible*, Springer, 2010 ("Kotler and Pfoertsch (2010)"), pp. 310-314.

[49]　Kotler and Pfoertsch (2010), p. 319.

Report amount to little more than subjective personal views about how Dr. Dhar believes the Arm brand might be perceived or whether the use of the Arm Trademarks might cause confusion. In other words, Dr. Dhar is asking us to accept his opinions simply because he says so.

IV.   THE DHAR REPORT OFFERS NO VALID SUPPORT IN ITS ASSESSMENT OF THE ARM BRAND AND ITS ASSESSMENT OF THE RELATIONSHIP BETWEEN THE ARM AND QUALCOMM BRANDS

37.   The Dhar Report looks at the Arm brand from two perspectives. First, it discusses the Arm brand as seen by its direct B2B customers (e.g. chip makers, electronics manufacturers).[50] Second, the report also refers to the brand as an ingredient brand (i.e., a brand whose inclusion as a component of another brand makes the later more attractive to downstream or end customers).[51] In this section, I examine the Dhar Report's discussion of the Arm brand from both perspectives.

38.   The Dhar Report's assessment of the purported strength of the Arm brand is incomplete and cannot be relied upon. The Dhar Report asserts that Arm "has a strong and distinctive B2B brand" without credible support.[52] Namely, the Dhar Report: (i) fails to provide any customer-based evidence of brand awareness or brand association; (ii) claims that the Arm brand serves as a strong ingredient brand without offering any rigorous assessment; and (iii) fails to take into consideration Qualcomm's own brand and brand strength in its relationship to Arm.

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[50]   *See*, *e.g.*, Dhar Report, ¶¶ 93-106.

[51]   Dhar Report, ¶ 105.

[52]   Dhar Report, Section VIII.B.

A. The Dhar Report Claims That Arm's Brand Is Strong Without Providing Evidence of Customers' Impressions of the Arm Brand

39.   As the Dhar Report (correctly) argues, strong brands are rooted in consumer memory. The knowledge of a brand stored in consumer memory "can be characterized in terms of two components: brand awareness and brand image.

- **Brand awareness** is related to the strength of the brand in memory, as reflected by consumers' ability to identify the brand under different conditions.

- **Brand image** is perceptions about a brand as reflected by the brand associations held in consumer memory."[53]

Strong brands have both strong awareness (or identification of the mark) with particular goods and/or services and a strong brand image in memory by having strong, favorable, and unique brand associations.[54]

40.   Such a characterization of brands and brand strength requires that any rigorous, scientifically valid assessment of brand strength must be based on what consumers hold in memory. In other words, the assessment must rest on customer-based analyses of brand awareness and brand associations. Such evidence of potential sources of brand equity may include results from qualitative and quantitative market research methods, such as customer

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[53]   Dhar Report, ¶ 87.

[54]   Dhar Report, ¶ 87-90. *See also*, *e.g.*, Kotler, Philip, and Kevin L. Keller, *Marketing Management*, Fifteenth Edition, Pearson, 2016 ("Kotler and Keller (2016)"), pp. 301-302 ("**Branding** is the process of endowing products and services with the power of a brand. It's all about creating differences between products. Marketers need to teach consumers 'who' the product is—by giving it a name and other brand elements to identify it—as well as what the product does and why consumers should care. Branding creates mental structures that help consumers organize their knowledge about products and services in a way that clarifies their decision making and, in the process, provides value to the firm […] **Brand equity** is the added value endowed to products and services with consumers. It may be reflected in the way consumers think, feel, and act with respect to the brand, as well as in the prices, market share, and profitability it commands.").

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surveys, brand recognition studies or ranking exercises, or brand association exercises.[55] Crucially, a brand analysis that concludes a brand is strong would only be scientifically valid if it includes some evidence of high awareness and positive brand associations among the customers for the brand being examined.

41.   The Dhar Report, however, includes no such customer-based analysis of Arm's brand strength. In fact, the Dhar Report section on Arm's strength as a brand includes no evidence *at all* from Arm's direct customers, let alone from Arm's downstream customers.[56] In fact, outside of the Dhar Report's citations to various trade awards won by Arm as a firm since 2010,[57] the only other sources the Dhar Report ties directly to claims about Arm's purported brand strength are public testimony of a current Arm executive and Arm's own 2023 Form F-1 company filing to the U.S. SEC.[58] These sources do not provide reliable evidence of relevant customers' awareness of or associations with the Arm brand.

42.   The lack of customer-based evidence is concerning given the Dhar Report's emphasis on the fact that "Arm is a B2B brand" with large, well-known customers in the tech industry.[59] For example, despite stating that "Arm's direct customers are chip developers and manufacturers, such as Amazon, Google, Intel, NVIDIA, and Samsung, rather than end

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[55]   Keller and Swaminathan (2020), pp. 332-366.

[56]   *See* Dhar Report, Section VIII.

[57]   *See* Dhar Report, ¶ 99.

[58]   *See* Dhar Report, ¶¶ 97-106; ARM_01259705–0105; Lardinois, Frederic, "Arm After the IPO," *TechCrunch*, September 14, 2023, available at https://techcrunch.com/2023/09/14/arm-after-the-ipo/ (quoting Will Abbey, Arm's Executive VP and Chief Commercial Officer).

[59]   Dhar Report, ¶ 97.

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customers,"[60] the Dhar Report draws no direct evidence from these customers in general

or any individuals who occupy a variety of roles in such companies (each with numerous

divisions and employees). The Dhar Report does not, for example, investigate how these

market participants experience the Arm brand in any level of detail, separate and apart from

the Dhar Report's earlier, general overview of Arm's licensing structure.[61]

43.   Further, the Dhar Report ignores the crucial question of business-customer and end-

consumer awareness. The Dhar Report presents various assertions toward Arm's purported

brand strength, such as "Arm offers benefits to downstream customers" or "Arm's

innovation is responsive to consumer demands," without any context or further evidence

collected from among the audience of relevant parties outside Arm for whom the Dhar

Report claims these brand assets are perceived.[62]

44.   The Dhar Report's lack of further evidence from outside Arm is noteworthy. For example,

the Dhar Report states that "[a] strong brand like Arm arises from the thoughts, feelings,

and associations that are linked to the Arm brand,"[63] yet does not provide any evidence of

these brand associations. The Dhar Report's failure to consider any outside evidence for its

conclusions renders the conclusions suspect, particularly given the many well-established

research methods available to assess the strength of a brand and customers' associations

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[60]   Dhar Report, ¶ 97.

[61]   *See* Dhar Report, ¶¶ 32-47.

[62]   Dhar Report, ¶¶ 103-104. The only evidence offered for these points are statements from Arm's own 2023
        SEC F-1 filing.

[63]   Dhar Report, ¶ 105.

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with the brand.[64] It was not impossible for Dr. Dhar to have collected and reviewed such data in the process of preparing his report.

45.   The non-customer evidence that the Dhar Report solely relies upon fails to fill the gap left by a lack of any business-customer and end-consumer evidence for Arm's purported brand strength. For example, the Dhar Report cites recognition of Arm by the World Intellectual Property Organization, Arm's sales and the prior year's inventory of Arm-based chips, and awards won by Arm between 2010 and 2021 as evidence that "[t]he Arm Trademarks have been strong and distinctive marks for decades."[65] In stating that these strands of evidence prove the Arm Trademarks' strength and distinctiveness, the Dhar Report does not explain whether: (1) the direct B2B and/or the downstream end-consumer audiences of Arm's brand are aware of any of this information; (2) whether awards won by Arm or the volume of sales of Arm-based products matter to these groups of customers, and if so, how; or even (3) whether Arm's recognition by award-presenting entities was based on any underlying information that would be relevant to purchasers of Arm's intellectual property. The Dhar Report's failure to tie these strands of evidence to perceptions among Arm's customers is critical, as the purported strength or distinctiveness of the Arm brand relies on consumer perceptions and not the evaluation criteria of various award-granting entities.[66] Were it the

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[64]   *See, e.g.*, Keller and Swaminathan (2020), pp. 332-366. For example, an introductory textbook on strategic brand management describes many qualitative research techniques (e.g., free association, adjective ratings, personification exercises) and quantitative techniques (e.g., direct and indirect measures of brand recognition, aided and unaided measures of brand recall, scale measures of brand attributes and benefits) to assess possible brand associations and the depth of customers' brand awareness. Keller and Swaminathan (2020), p. 360.

[65]   Dhar Report, ¶ 99.

[66]   Elsewhere, in its abstract discussion of brand strength, the Dhar Report recognizes that promotional efforts and media coverage surrounding the brand inform consumer impressions of the brand, yet the Dhar Report

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case, for example, that any of these accolades do indeed inform business customers and end consumers' brand perceptions of Arm, it would be Dr. Dhar's responsibility as a researcher to draw out and demonstrate any such associations, instead of merely listing inventory figures and third-party recognitions of Arm and implying that they are of constituent importance to Arm's brand strength amid a lack of direct, consumer-based evidence.

46.   Instead, the Dhar Report's attempted evaluation of Arm's brand strength reflects merely the *goals* of Arm's branding efforts and does not interrogate the extent to which those branding efforts are successful. Such an evaluation would require customer-based evidence. For example, the Dhar Report cites the company's 2023 SEC F-1 filing to support the statement that "[t]he value that the Arm Trademarks communicate to its customers is based on the pervasiveness and differentiating features of its CPU and ISA [instruction set architecture] offerings."[67] The Dhar Report does not provide any evidence that the Arm brand actually has this differentiating impact in the real world (i.e., as a perception among Arm's real, existing customers).

47.   The Dhar Report further states that "[b]eyond building its brand through its performance and partnership with reference customers, Arm has worked to develop its brand among the relevant pool of potential buyers in other ways[,]" including industry events and company-

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performs no analysis to show how the awards won by Arm have informed consumer impressions of Arm's brand. *See* Dhar Report, ¶ 81 ("Second, a brand name and other brand identity elements take on meaning to customers based on repeated experience with the brand as well as from its advertising/promotional efforts and profile in the media.").

[67]   Dhar Report, ¶ 98.

led webinars.[68] The Dhar Report presents no evidence that would show the extent to which these efforts are or have been effective, and the Dhar Report fails to provide any evidence of the Arm brand's broad recognition among the relevant audience. Instead, the Dhar Report merely describes how Arm theoretically, and ideally, would be perceived if Arm's brand-building efforts are a success.

48.   In sum, the sources cited in the Dhar Report do not shed light on what actual or potential purchasers of Arm's intellectual property understand the Arm brand to mean.

B.   The Dhar Report Offers No Evidence to Support Its Description of Arm as a Strong "Ingredient Brand"

49.   The Dhar Report repeatedly suggests that products linked to Arm benefit from Arm's brand strength as an ingredient brand,[69] but the Dhar Report fails to provide any analysis of Arm *as an* ingredient brand. For example, the Dhar Report defines ingredient branding as "a type of co-branding or a process in which a company markets an established branded ingredient or component used in its own products" and suggests that this marketing strategy "seeks to signal the benefits built on the strong and favorable brand identity of the ingredient (e.g., Arm in this case)."[70] Yet, the Dhar Report does not analyze Arm as an ingredient brand either in relation to the end-consumers who purchase the end product or

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[68]   Dhar Report, ¶ 100.

[69]   *See* Dhar Report, ¶ 83, 105. *See also* Dhar Report, ¶¶ 87, 90.

[70]   Dhar Report, ¶ 83.

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in relation to industrial customers that operate in Arm's B2B market — where an ingredient brand's measurable performance and quality are of utmost importance.[71]

50.   Ingredient branding is indeed a strategy that identifies the specific brand of individual components (or "ingredients") of a product or service in an effort to convey a differentiated value to customers,[72] and ingredient branding can be an important analytical approach to understand marketing efforts along a complex, industrial supply chain. For example, in the chip industry, ingredient branding may be used to distinguish brand identities to end consumers among the various parties overlappingly involved in licensing, designing, testing, or manufacturing chips, integrating those chips into a larger product (such as a laptop), and marketing and selling these products to retailers and consumers.

51.   The computing industry in particular has seen many component manufacturers aiming to replicate the success of the "Intel Inside" ingredient branding campaign.[73]

52.   When "Intel Inside" launched in 1991, the Intel brand, which "had been largely unknown to consumers," became a way for a non-technical audience to "understand that their devices contained quality components provided by the company that defined the state of the art."[74]

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[71]   [redacted]

[72]   Kotler and Pfoertsch (2010), pp. 2-5, 16-19.

[73]   *See*, *e.g.*, Kotler and Pfoertsch (2010), p. 93. ("AMD, MSI, ATI and NVIDIA (CPU, main board and graphic cards manufacturers) […] have succeeded in securing partnership agreements with PC manufacturers to have their logos shown on the computers. They also convinced the retailers and final users that their component is superior and makes a difference for them.")

[74]   "Ingredient Branding: End User Marketing and 'Intel Inside,'" *Intel*, available at https://www.intel.com/content/www/us/en/history/virtual-vault/articles/end-user-marketing-intel-inside.html, accessed on February 12, 2024. *See also* Kotler and Keller (2016), p. 389 ("Many

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The "ingredient" that launched Intel's campaign was its 386 microprocessor, which represented a "major technological breakthrough" — at least to industry experts in the know — but which initially lagged in sales.[75] Intel executives pioneered a campaign to educate end consumers about the premium benefits of Intel's new chip while simultaneously convincing its direct-customer original equipment manufacturers ("OEMs") to append the "Intel Inside" logo to products containing the chip. The final result was an unprecedented instance of lay consumer brand association with a component computer product (i.e., an ingredient) driving upstream sales.[76]

53.   The Dhar Report opines that "Arm offers benefits to downstream customers" and that "[t]he strength of the Arm brand means that products that are linked to Arm (e.g., as an ingredient of the product) are conferred positive associations that have been developed by the Arm

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manufacturers make components or materials that enter final branded products but lose their individual identity. One of the few companies that avoided this fate is Intel. Intel's consumer-directed brand campaign convinced many personal computer buyers to buy only brands with 'Intel Inside.' As a result, major PC manufacturers—Dell, HP, Lenovo—typically purchase their chips from Intel at a premium price rather than buy equivalent chips from an unknown supplier."); Kotler and Pfoertsch (2010), pp. 59-60 ("Although [Intel] was widely recognized among computer manufacturers, the brand had little name recognition amongst end users, despite the fact that Intel microprocessors were the 'brains' inside their PCs […]." "The key to this [ingredient branding] strategy was gaining consumer's confidence in Intel as a brand and demonstrating the value of buying a microprocessor from the industry's leader and the pioneer of the microprocessor.").

[75] "Ingredient Branding: End User Marketing and 'Intel Inside,'" *Intel*, available at https://www.intel.com/content/www/us/en/history/virtual-vault/articles/end-user-marketing-intel-inside.html, accessed on February 12, 2024.

[76] "Ingredient Branding: End User Marketing and 'Intel Inside,'" *Intel*, available at https://www.intel.com/content/www/us/en/history/virtual-vault/articles/end-user-marketing-intel-inside.html, accessed on February 12, 2024. *See also* Kotler and Pfoertsch (2010), p. 63 ("However, by 2002, the Intel Inside initiative had become one of the world's largest cooperative marketing programs with over 1,000 PC makers using the logo (a total of 2,700 computer makers licensed). Intel and other companies had spent over $4 billion on advertising since the slogan was launched in 1991, and the Intel brand had been ranked many times as one of the top 10 best-known brands in the world."); Kotler and Pfoertsch (2010), p. 69 ("The implementation of the [Intel Inside] Ingredient Branding concept resulted in an unprecedented business success and changed the industry structure.").

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brand over the years of successful innovation."[77] The Dhar Report further opines that as a result "Qualcomm's unauthorized use of Arm's Trademark in connection with the Nuvia Products will likely divert sales from authorized users of Arm's Trademark."[78]

54.   The Dhar Report does not apply to its analysis of Arm's brand any established marketing knowledge or literature about what constitutes a successful ingredient brand. For example, Kotler and Pfoertsch's textbook on ingredient branding identifies several approaches for assessing the value of ingredient brands, such as applying methods to assess brand equity, brand loyalty, brand trust, brand awareness, recognized quality, and brand associations.[79] For instance, a successful ingredient brand is one for which its consumers "believe the ingredient matters to the performance and success of the end product," and where consumers are "convinced that not all ingredient brands are the same and that the ingredient is superior."[80] Further, consumers "do not necessarily have to know exactly how the ingredient works—just that it adds value."[81] For instance, to measure what that value is and "measur[e] Ingredient Branding success" "at this [B2B] stage, it is recommended that a financially oriented measurement tool based on price premiums be used."[82]

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[77]   Dhar Report, ¶¶ 103, 105.

[78]   Dhar Report, ¶ 132.

[79]   Kotler and Pfoertsch (2010), pp. 310-314.

[80]   Kotler and Keller (2016), p. 390.

[81]   Keller and Swaminathan (2020), p. 277.

[82]   Kotler and Pfoertsch (2010), p. 319.

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55.   By failing to provide any end-customer-based evidence of Arm's strength as an ingredient

        brand or apply any established marketing criteria or method, the Dhar Report fails to

        establish reliable foundations for its conclusions on Arm's strength as an ingredient brand.

56.   Instead of providing end-customer-based evidence, the Dhar Report states without support

        that "products that are linked to Arm (e.g., as an ingredient of the product) are conferred

        positive associations that have been developed by the Arm brand over the years of

        successful innovation."[83] Dr. Dhar does not offer any specific evidence for how Qualcomm

        or any of Arm's other industrial customers benefit from the (undemonstrated) strength of

        Arm as an ingredient brand in their products. Further, despite stating that a brand's

        "mentions as an ingredient of the product by the licensee and media are important factors

        in establishing brand awareness and a brand image,"[84] the Dhar Report contains no analysis

        on whether this is the case for Arm. Indeed, the Dhar Report offers no evidence that Arm

        has taken any affirmative steps to market itself as an ingredient brand. Far from Intel's

        campaign to instill the value of Intel technology in the minds of consumers, the Dhar Report

        does not point to *any* consumer-facing advertisements by Arm, let alone a sustained effort

        to establish itself as an ingredient brand.

57.   Without any customer-based analysis or application of established marketing knowledge

        to assess the success of an ingredient brand, the Dhar Report cannot establish that the Arm

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[83]   Dhar Report, ¶ 105. *See also* Dhar Report, ¶ 97 ("Arm's offerings […] enable its licensees to develop,
       manufacture, and sell a wide range of technology products—including smartphones, tablets and personal
       computers, data centers and networking equipment, vehicles, smartwatches, thermostats, and drones and
       industrial robotics—to their own customers.").

[84]   Dhar Report, ¶ 87.

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brand is a strong ingredient brand in either Arm's B2B market or, ultimately, in end-consumers' decisions to purchase an Arm-based end product.

C. The Dhar Report Fails to Consider the Extent to Which Qualcomm's Brand Plays a Role in Marketing Qualcomm's Arm-based Products to Consumers

58.   The Dhar Report's implication that Arm's brand is an ingredient in the overall success of end products among downstream consumers fails to consider the potentially significant role of other brands and brand components, including Qualcomm's, in these end products' marketing or commercial success. In particular, the Dhar Report neglects whether end consumers (i.e., consumers who purchase end products with Arm-compatible chips) are provided with any information about Arm when making their purchases of products with Arm-based technologies, and whether these efforts, to the extent they occur, are effective. This immediately raises the question as to whether the Arm brand could possibly have high end-consumer awareness.

59.   Furthermore, the Dhar Report fails to consider the potentially important role of Qualcomm's own brand in the marketing of Qualcomm OEM products. It devotes no attention at all to how Qualcomm markets its OEM products.

60.   Qualcomm presumably has its own (arguably strong) brand reputation in the relevant marketplace, and would similarly "impact consumer purchase behavior," "take on meaning to customers based on repeated experience with the brand," and "serve to reduce the risk associated with product purchase decisions,"[85] as the Dhar Report describes in its own rubric for a theoretical strong brand. The Dhar Report, however, contains no analysis of the

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[85]   Dhar Report, ¶¶ 80-82.

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interplay between Arm's branding and the OEMs who offer final products that result, in some form, from a relationship with Arm. Such an analysis is needed as it may be the case that Qualcomm's brand, and the brands of other Arm B2B customers, are more recognizable among relevant end-consumers than Arm's. For example, Qualcomm's brand, and in particular the logo and branding of its Snapdragon product line, is often prominently displayed on certain products that are marketed as containing Qualcomm components.[86] Further, Qualcomm's Snapdragon brand has also been prominently featured in promotional imagery for Samsung phones, the second-best-selling smartphone brand in the U.S.,[87] and in connection with Lenovo laptops, as shown in **Figure 1** and **Figure 2** below.

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[86]   *See, e.g.*, "'HP Laptop 14" FHD, Touch, Qualcomm Snapdragon 7c Gen 2, 4GB RAM, 128 GB eMMC, Silver, Windows 11, 14-ed0123wm,'" *Walmart*, available at https://www.walmart.com/ip/HP-Laptop-14-FHD-Touch-Qualcomm-Snapdragon-7c-Gen-2-4GB-RAM-128-GB-eMMC-Silver-Windows-11-14-ed0123wm/185295507, accessed on February 19, 2024; "Acer Chromebook Spin 513," *Acer*, available at https://www.acer.com/us-en/chromebooks/acer-chromebook-spin-513-cp513-1h-cp513-1hl-r841lt-r841t, accessed on February 19, 2024; "Meet Galaxy Book Go," *Samsung*, available at https://www.samsung.com/us/app/computing/galaxy-book-go/, accessed on February 19, 2024; "Snapdragon for Inspiron 14," *Dell*, available at https://www.dell.com/en-us/lp/qualcomm-snapdragon, accessed on February 19, 2024.

[87]   "Manufacturers' Market Share of Smartphone Sales in the United States from 1st Quarter 2016 to 2nd Quarter 2023," *Statista*, October 27, 2023, available at https://www.statista.com/statistics/620805/smartphone-sales-market-share-in-the-us-by-vendor/.

Figure 1. Qualcomm Snapdragon Branding Elements in Promotional Imagery for

Samsung Galaxy Phones[88]

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[88]   @SamsungMobile, "Battle your way to victory with the upgraded Snapdragon® 8 Gen 2 Mobile Platform. 🎮 #GalaxyZFold5 #JoinTheFlipSide #SamsungUnpacked," *X*, available at https://x.com/samsungmobile/status/1684163305437532160?s=51, accessed on February 19, 2024.

Figure 2. Qualcomm Snapdragon Branding Elements in Promotional Imagery for

Lenovo ThinkPad Laptops[89]

61.   By failing to include any analysis of the ecosystem of other brands that surround Arm and

Arm's technologies, the Dhar Report cannot, for example, disentangle any brand

associations customers might (or might not) hold for Arm from those that they might hold

for other parties, among the relevant industrial and/or end-consumer audience. Further, the

Dhar Report fails to consider that, due to Qualcomm's own brand positioning, it may be

the case that Qualcomm could further Arm's objective to build a strong brand. As such, the

Dhar Report cannot rule out, for example, that Qualcomm's own marketing could add to

any goodwill associated with the Arm brand and the Arm Trademarks rather than detract

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[89]   "ThinkPad X13s Snapdragon (13")," *Lenovo*, available at
https://www.lenovo.com/us/en/p/laptops/thinkpad/thinkpadx/thinkpad--x13s-(13-inch-
snapdragon)/21bx0008us?orgRef=https%253A%252F%252Fwww.google.com%252F, accessed on
February 19, 2024.

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from it, and his conclusion that end products "are conferred positive associations" due to the "strength of the Arm brand" lack context informed by the real-world industry and are wholly unsupported.[90]

62.   In sum, the Dhar Report fails to put forward a rigorous analysis of the Arm brand through any of: (1) an established and replicable empirical framework, (2) the employment of neutral, empirical, and consumer-based evidence, and (3) an appropriately defined context for Arm's brand strength within the relevant industry. As a result, the Dhar Report merely assumes the strength of the Arm brand.

V.   THE DHAR REPORT'S ASSERTION THAT QUALCOMM'S USE OF THE ARM TRADEMARKS IS LIKELY TO CAUSE CONFUSION IS BASELESS

63.   The Dhar Report concludes that "Qualcomm's use of Arm's Trademarks is likely to cause customer confusion" and "is likely to mislead customers and other relevant industry participants into believing that there is some connection as to source, affiliation, sponsorship, or approval between Arm and Qualcomm."[91] These conclusions are baseless for several reasons. *First*, the Dhar Report inappropriately points to Qualcomm's historical uses of the Arm Trademarks to assume that Qualcomm will likely use the Arm Trademarks in the same way in the future. *Second*, the Dhar Report's conclusions regarding confusion are flawed because the Dhar Report fails to consider the sophistication of the B2B industrial procurement departments that purchase Qualcomm's chips, which are highly trained and

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[90]   Dhar Report, ¶ 105 ("The strength of the Arm brand means that products that are linked to Arm (e.g., as an ingredient of the product) are conferred positive associations that have been developed by the Arm brand over the years of successful innovation.").

[91]   Dhar Report, ¶ 15.

may therefore be unlikely to be confused by uses of the Arm Trademarks to describe Qualcomm custom cores' technical attributes. *Third*, the Dhar Report's assertion that Qualcomm's purported use of the Arm Trademarks creates a false understanding of the custom cores' affiliation, sponsorship, or certification is unsupported. *Fourth*, the Dhar Report presents no evidence of any actual confusion caused by Qualcomm's purported use of the Arm Trademarks, and the report overlooks admissions by Arm and testimony from Arm's corporate deponents that indicate that Arm itself has been unaware of any actual confusion.

A. The Dhar Report Fails to Consider That Qualcomm's Purportedly Infringing Use of the Arm Trademarks Is Distinct from Qualcomm's Historical Uses of the Arm Trademarks

64.   The Dhar Report offers the unfounded opinion that "Qualcomm's prior history and usage of Arm's Trademarks, along with requirements in the relevant agreements and materials that it will provide to customers, demonstrate a *high likelihood* (emphasis added) that Qualcomm will continue to use Arm's Trademarks in connection with its future products, particularly Nuvia Products."[92] The Dhar Report inappropriately assumes that past usage indicates future usage, particularly under different circumstances. In particular, the Dhar Report's conclusion that Qualcomm's use of the Arm Trademarks is likely to create confusion is partly based on the Dhar Report's analysis of Qualcomm's prior use of the Arm Trademarks in connection with Arm-built CPU cores, rather than Qualcomm's *custom-designed* cores that are compatible with the Arm ISA.

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[92]   Dhar Report, ¶ 14 (emphasis added).

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65. Specifically, the Dhar Report points to the following examples[93] of historical Qualcomm uses of Arm Trademarks, which relate to *Arm-built cores* licensed by Qualcomm under its TLA:

    a. A 2022 Qualcomm Application Processors Selector Guide, which describes technical specifications for certain Qualcomm SoCs in the Internet of Things ("IoT") segment (e.g., the Qualcomm® APQ8053Pro, which is described as having a "8x Arm Cortex A53 CPU");[94]

    b. A September 2016 Device Specification for Qualcomm's Snapdragon 410E (APQ 8016E) processor, which describes the technical specifications of this processor as having an "ARM Cortex-A53" CPU.[95]

    c. A 2022 article published online in *Business Insider India* about the Qualcomm 2022 Tech Summit and the Kryo CPU, which the article notes was built "on the latest ARM-V9 architecture."[96]

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[93] The Dhar Report additionally points to a February 2022 press release "published in relation to the 2022 Mobile World Congress event," which makes general statements about the "Arm®-based Snapdragon computing ecosystem" and which suggests "[t]ogether with Qualcomm Technologies, global OEMs deliver Windows 11 on Arm PCs." *See* Dhar Report, ¶ 111. This use of "Arm-based" strikes me as consistent with the instructions found in the "Referential use of Arm's trademarks" section of Arm's publicly-available Trademark Use Guidelines (which I discuss in more detail in Section V.C) and merely refers to the Arm Trademarks to describe the ISA that Qualcomm's custom core chip implements.

[94] Dhar Report, ¶ 107, citing "Qualcomm Application Processors Selector Guide," *Qualcomm,* 2022, available at https://www.qualcomm.com/content/dam/qcomm-martech/dm-assets/documents/application-processors-selection-guide.pdf.

[95] Dhar Report, ¶ 108, citing "Qualcomm® Snapdragon 410E (APQ 8016E) Processor Device Specification," *Qualcomm*, September 2016, available at https://www.qualcomm.com/content/dam/qcomm-martech/dm-assets/documents/snapdragon_410e_apq_8016e_data_sheet.pdf.

[96] Dhar Report, ¶ 109, citing Jain, Sourabh, "Qualcomm Snapdragon Tech Summit 2022 — Snapdragon 8 Gen 2, Oryon CPU, AR2 Gen 1 Platform, and Other Announcements," *Business Insider India*, November 17, 2022, available at https://www.businessinsider.in/tech/news/qualcomm-snapdragon-tech-summit-2022-snapdragon-8-gen-2-oryon-cpu-ar2-gen-1-platform-and-other-announcements/articleshow/95581109.cms.

    d. A 2023 "Snapdragon 8 gen 3 Mobile Platform Product Brief,"[97] which describes the technical specifications of the Qualcomm Kryo CPU as containing "Arm Cortex-X4 technology."[98]

66.   Notably, I understand that these "historical" uses cited in the Dhar Report (with the exception of the *Business Insider India* article)[99] are focused on the use of Arm as a source-designator: they tell consumers that the Qualcomm product contains a specific type of *Arm-built core*. However, when Qualcomm markets *its own, custom cores*, which are compatible with the Arm ISA, the company is marketing a different offering that does not leverage Arm-built cores.[100] The Dhar Report ignores the fact that this different use would in fact likely lead to different marketing strategies. In particular, the Dhar Report ignores that Qualcomm currently uses the Arm Trademarks in connection with its custom cores to *refer*

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[97]   Dhar Report, ¶ 110, citing "Snapdragon® 8 Gen 3 Mobile Platform," *Qualcomm*, October 23, 2023, https://docs.qualcomm.com/bundle/publicresource/87-71408-1_REV_B_Snapdragon_8_gen_3_Mobile_Platform_Product_Brief.pdf.
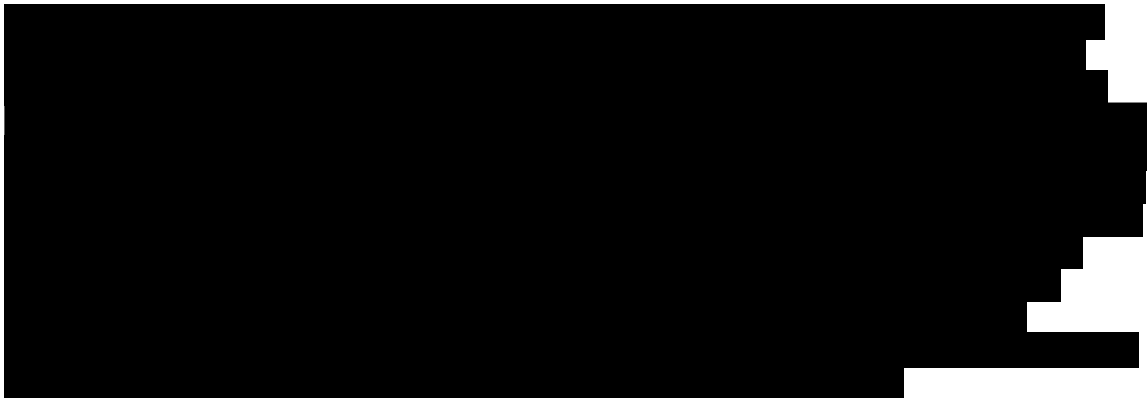
[98]   Dhar Report, ¶ 110, citing "Snapdragon® 8 Gen 3 Mobile Platform," *Qualcomm*, October 23, 2023, https://docs.qualcomm.com/bundle/publicresource/87-71408-1_REV_B_Snapdragon_8_gen_3_Mobile_Platform_Product_Brief.pdf.

[99]   The Dhar Report mischaracterizes the *Business Insider India* source by claiming "[at] Qualcomm's 2022 Tech Summit, it announced that its Kryo CPU will be 'built on the latest ARM-V9 architecture,'" which suggests Qualcomm itself produced that quote. In reality, it was the author of the article who wrote "[t]he Snapdragon 8 Gen 2 chipset is equipped with the new Kryo CPU built on the latest ARM-V9 architecture." It is not clear from the source cited in the Dhar Report how Qualcomm used the Arm Trademarks if at all in its announcement at its 2022 Tech Summit. *See* Dhar Report, ¶ 109, citing Jain, Sourabh, "Qualcomm Snapdragon Tech Summit 2022 — Snapdragon 8 Gen 2, Oryon CPU, AR2 Gen 1 Platform, and Other Announcements," *Business Insider India*, November 17, 2022, available at https://www.businessinsider.in/tech/news/qualcomm-snapdragon-tech-summit-2022-snapdragon-8-gen-2-oryon-cpu-ar2-gen-1-platform-and-other-announcements/articleshow/95581109.cms.

[100]   *See, e.g.,* "Qualcomm Announces Next-Generation Snapdragon Mobile Chipset Family," *Qualcomm*, February 13, 2011, available at https://www.qualcomm.com/news/releases/2011/02/qualcomm-announces-next-generation-snapdragon-mobile-chipset-family. *See also* ARM_00088656–684 at 662, 671 (explaining that "architectural licensees do *not* use Arm's CPU designs," but rather "create their *own* proprietary CPU designs using their *own* engineering teams," and that, as a result, architectural licensees' CPU designs compete against Arm-built "off-the-shelf" CPU implementations. Emphasis in original.).

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to the technical capabilities of its products.[101] That is, Qualcomm does not purport to use

the "Arm" word mark to indicate that a certain Arm core is being used, but rather only to

provide a description of the technical attributes of the product — that the core is compatible

with the Arm ISA.

67.   The Dhar Report does not appear to dispute that Qualcomm's current use of the Arm

Trademarks in connection with Qualcomm's publicly announced custom cores are limited

to uses such as "Arm-based," "Arm-compatible," or "Arm-compliant." The Dhar Report

cites to only two examples[102] of any Qualcomm marketing materials using the Arm word

mark (and <u>none</u> using the Arm logo) in connection with public descriptions by Qualcomm

pertaining to its custom core technologies — the *only* technologies that I understand are at

issue in this litigation:

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[101]   ██

[102]   I note the Dhar Report cites three sources relating to Qualcomm's current use of the Arm Trademarks.
However, because the first of the three, a Qualcomm press release published on January 3, 2022 stating
there is "broad support from ecosystem partners for the PC industry's transition to Arm®-based
computing," and that Qualcomm's "acquisition of NUVIA uniquely positions Qualcomm Technologies to
drive this industry wide transition," was published prior to the announcement of Qualcomm's first custom
core (the Qualcomm Oryon Custom Core), it is therefore more accurately considered a historical use of the
Arm Trademark. I further note that the Dhar Report cites a press release that was published *after* the
January 3, 2022 press release as a *historical* use of the Arm Trademark, which further supports its
classification as also an instance of historical use. *See* Dhar Report, ¶¶ 112(a), 111.

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a. "At Qualcomm's 2023 Snapdragon Summit, Director of Product Management Manju Varma announced that the Oryon CPU would be the first 'CPU on Arm-based architecture to hit over 4GHz,'[103] and

b. "On Qualcomm's November 1, 2023, Earnings Call, Qualcomm CEO Cristiano Amon explained the Snapdragon X Elite 'Arm-based PC processor … is going to be part of the expansion of TAM [Total Addressable Market] for Qualcomm[.]'"[104]

68. These uses of the Arm Trademarks are distinguished from the Dhar Report's citations of Qualcomm's historical uses of the Arm Trademarks in that they incorporate a modifier like "-based," "-compliant," or "-compatible" and are used in factually accurate statements about Qualcomm's products — not as a branding description of the product itself.[105] The Dhar Report does not address this distinction whatsoever; nor does it offer any empirical evidence on how relevant B2B customers understand or perceive the terms "Arm-based," "Arm-compliant," or "Arm-compatible." The Dhar Report simply ignores that Qualcomm's uses of the Arm Trademarks in connection with the Qualcomm custom cores may be referential only. "Referential use," as I use it in this report, describes situations in which someone uses a term (which can be a trademark) to *refer to* or describe a product or

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[103] Dhar Report, ¶ 112(b), citing ARM_01422901 at 37:32.

[104] Dhar Report, ¶ 112(c), citing "Qualcomm (QCOM) Q4 2023 Earnings Call Transcript," *The Motley Fool*, September 30, 2023, available at https://www.fool.com/earnings/call-transcripts/2023/11/01/qualcomm-qcom-q4-2023-earnings-call-transcript/.

[105] The other examples cited in the Dhar Report of statements by Qualcomm concerning its development of the Qualcomm custom cores focus on the use of the term Nuvia – not the use of the Arm Trademarks. For example, the Dhar Report cited Qualcomm statements that, by "late next year, beginning 2024, you're going to see Windows PCs powered by Snapdragon with a *Nuvia-designed CPU*," and that "the creation of our custom CPU was *started by Nuvia engineers while employed at Nuvia*" (emphasis added). *See* Dhar Report, ¶ 116. The Dhar Report purports that this would confuse the sophisticated purchasers of Qualcomm's products about the "sponsorship, affiliation, or certification of the Nuvia Products by Arm," but cites no evidence or methodology to support this statement.

service in a manner that aids identification.[106] As I will discuss in more detail in **Section V.C** below, Qualcomm's uses of the Arm Trademarks in connection with Qualcomm *custom cores* to *refer* to the technical capabilities of Qualcomm's products are different from Qualcomm's prior uses of the Arm Trademarks in connection with other Qualcomm products that use *Arm-built cores* licensed by Qualcomm.

69.   The Dhar Report overlooks this critical distinction, provides no basis for arguing that Qualcomm's future uses of the Arm Trademarks will be anything other than referential, and consequently has no scientific basis from which to assert that Qualcomm's use of the Arm Trademarks are likely to cause confusion.

B. The Dhar Report's Analysis of Confusion Fails to Take into Account That Arm Operates in a Business-to-Business Market Where Customers Are More Sophisticated Than General Consumers and Therefore Less Likely to Be Confused

70.   The Dhar Report fails to factor in the unique context of B2B transactions within the chip industry. Despite acknowledging the sophistication of both Arm's and Qualcomm's B2B customers,[107] the Dhar Report fails to adequately address this aspect, leading to a conclusion that lacks credibility. Consequently, its assertion regarding the likely confusion caused by Qualcomm's use of the term "Arm-based" or "Arm-compliant" among sophisticated and knowledgeable procurement professionals, such as engineers, is

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[106]   I understand there is a legal application of the term "referential use" that has similarities with my use of the term. *See, e.g.*, "Fair Use of Trademarks (Intended for a Non-Legal Audience)," *International Trademark Association*, December 16, 2020, available at https://www.inta.org/fact-sheets/fair-use-of-trademarks-intended-for-a-non-legal-audience/.

[107]   *See* Dhar Report, ¶ 95 ("B2B products are generally purchased by a group within an organization rather than a single individual, and as such can be subject to complex within-firm restrictions and negotiations."), citing Kotler, Philip, and Waldemar Pfoertsch, *B2B Brand Management*, Springer, 2006 ("Kotler and Pfoertsch (2006)"), p. 24.

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unfounded. Furthermore, the Dhar Report's failure to conduct an empirical analysis of customer confusion, particularly within the relevant market of purchasers, highlights the lack of concrete support for its conclusions and, as such, leaves us no choice but to simply accept his word for it.

71.   Industrial Marketing is the marketing of goods and services by one business to another, often referred to as business-to-business or "B2B" marketing. Compared to broader consumer audiences for final products, customers in a business-to-business, industrial marketplace are highly sophisticated and technically competent: they can be expected to evaluate and understand marketing statements in the context of the relevant industry.[108] B2B marketing is a long-term process that includes a great deal of scrutiny, close supplier-customer relationships, and often significant exchanges of money,[109] and therefore offers less potential for confusion, compared to marketing for end consumers.

72.   Procurement departments in the engineering sector often include engineers focused on defining the parameters of components they need in order to bring their ultimate product to market.[110] In this context, the component (such as an engine for a car) is not purchased based just on brand strength — rather, it is often the case that procurement decisions are about the ability to hit tightly-defined engineering objectives that focus on how the

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[108]   Kotler and Keller (2016), pp. 191-192. *See also* Turley, Lou, and Scott Kelley, "A Comparison of Advertising Content: Business to Business Versus Consumer Services," *Journal of Advertising*, Vol. 26, No. 4, 1997, pp. 39-48, p. 40 ("For example, business-to-business services have several distinctive characteristics that may differentiate them from consumer services… such as a more rational buying process, longer term relationships, greater product complexity, larger amounts of money exchanged, greater use of group decision making, and the design of customized service mixes unique to particular organizations.").

[109]   Kotler and Keller (2016), pp. 191-192.

[110]   Kotler and Keller (2016), pp. 192, 199.

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component will fit into the final product. Whether a component (the engine) is from company A or B may not matter as much in a B2B setting as a brand in a B2C setting, so long as the parameters are right and the component fits precisely (that is, the engine has the right technical specifications for that particular car).[111] The concept of interoperability is key — the component needs to be able to work (and work well) within the larger product in order to bring that product to market.[112] To determine interoperability, the engineers involved in the procurement process are likely to assess the technical specifications, and will usually test the performance of the components as well.[113]

73.   While the Dhar Report does not describe this process in detail, it recognizes that Arm and Qualcomm operate in a business-to-business market — and that customers in such markets are highly sophisticated. For example, the Dhar Report acknowledges that "[t]he products sold by B2B firms are often more complex, and buying transactions often involve significant technical expertise on both sides."[114] In a market such as that described in the

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[111]   For example, the start-up car manufacturer INEOS chose to fit its flagship model, the Grenadier, with a BMW-sourced engine, noting that the engine's impressive performance and reliability fit its design requirements nicely. *See* "Building the Grenadier: Episode 5 – Engine and Transmission," *INEOS*, available at https://ineosgrenadier.com/en/us/explore/the-grenadier-videos-and-stories/building-the-grenadier/engine-and-transmission, accessed on February 14, 2024.

[112]   Wegner, Peter, "Interoperability," *ACM Computing Surveys (CSUR)*, Vol. 28, No. 1, 1996, pp. 285-287, at p. 285 ("Interoperability is the ability of two or more software components to cooperate despite differences in language, interface, and execution platform.")

[113]

[114]   Dhar Report, ¶ 95, citing Kotler and Pfoertsch (2006), p. 21.

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Dhar Report, the important consideration for confusion is whether a chip-industry business-to-business customer (such as a decision-maker or procurement manager at Samsung) and not any specific individual or, importantly, end consumers, is likely to be confused by Qualcomm's purported use of the Arm Trademarks. The Dhar Report fails to examine likelihood of confusion through this lens; it does not analyze whether Qualcomm's actual customers (or similar market participants) are likely to be confused by Qualcomm's purported use of the Arm Trademarks.

74.   The Dhar Report does not grapple at all with the sophistication of the B2B procurement process in the industrial space. It does not even once mention the corporate procurement departments or the types of factors they consider in their purchasing decisions. Though the Dhar Report acknowledges that "buying transactions [between B2B firms] often involve significant technical expertise on both sides,"[115] it does not expand upon what "technical expertise" means, nor does it mention that there are often embedded engineers in procurement departments that influence purchasing decisions.[116] Further, the Dhar Report does not identify what information is likely to be relevant to those engineers in evaluating chip technology and ultimately in making purchasing decisions.

75.   To analyze whether the relevant audience for Qualcomm's marketing communications (i.e., industrial procurement specialists) are, in fact, likely to be confused by Qualcomm's

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[115] Dhar Report, ¶ 95.

[116] *See*, *e.g.*, "Senior Manager, Sourcing," *Qualcomm*, available at https://careers.qualcomm.com/careers/job/446697478074, accessed on February 26, 2024. Key responsibilities for this position within Qualcomm include "[w]ork with cross functional teams, external manufacturing partners and suppliers to ensure availability of Test Equipment and Hardware for engineering builds and high-volume production" and "[w]ork with product test engineering to define Test roadmaps and drive suppliers to deliver to Qualcomm's specification."

purported use of the Arm Trademarks, I would have expected Dr. Dhar to conduct a survey or other empirical analysis to produce customer-based evidence to support its statements about the likelihood of confusion concerning Qualcomm's purported use of the Arm Trademarks. Its failure to produce such empirical customer-based evidence is inconsistent with Dr. Dhar's prior practices.[117] The Dhar Report presents no evidence that any empirical analysis of relevant personnel at companies that procure chips or other relevant industrial products was conducted to determine whether Qualcomm's use of the Arm Trademarks to describe attributes of its own products is likely to be confusing. In fact, it is likely that these specialist purchasers of Qualcomm's products would view a term such as "Arm-based" as an indication of the technical attributes of the chip, rather than as an indicator of source.[118] Similarly, it does not determine whether the B2B purchasers of Qualcomm's products would even look at the types of marketing materials cited in the Dhar Report when making purchasing decisions, or whether they would instead rely on other sources of information.

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[117]   I am aware of prior instances in which Dr. Dhar has indeed used surveys or other empirical analyses to support his expert opinions on trademark infringement and likelihood of confusion with customer-based evidence. For example, in February 2016, Dr. Dhar submitted an expert report on behalf of Chrysler Group in the *Moab Industries v. Chrysler Group* matter, for which he conducted a likelihood of confusion survey. Dr. Dhar found that "the level of confusion between the MOAB INDUSTRIES word mark and Chrysler Group's MOAB mark used in connection with the Jeep brand is de minimis when tested in realistic marketplace conditions." Further, Dr. Dhar's opinions drew on the marketplace realities for the relevant consumers of a high-involvement good like a new car: "In summary, the higher involvement in the purchase decision will lead to consumers exercising a very high degree of care in gathering information on the purchase including that of source of the goods purchased." *See* Expert Report of Ravi Dhar, *Moab Industries, LLC. v. Chrysler Group LLC,* C.A. No. 3:12-cv-08247-HRH, United States District Court for the District of Arizona, March 7, 2014, ¶¶ 14, 50. Dr. Dhar chose not to conduct any type of similar, customer-based analysis in the course of preparing the present Dhar Report.

[118]   ██

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76.   Without adequately considering the critical context of B2B transactions in the relevant chip industry or offering concrete evidence of actual or potential confusion, the Dhar Report lacks any basis for its argument that the mere use of the term "Arm-based" or "Arm-compliant" is likely to be confusing to those sophisticated procurement professionals, including engineers. Because the Dhar Report acknowledges, but completely disregards, the sophistication of Arm's and Qualcomm's customers, its conclusion that purchasers would likely be confused lacks basis and credibility. Further, the Dhar Report's failure to undertake any defensible analysis of consumer confusion at all underscores that its opinions are factually and methodologically unsupported.

C. The Dhar Report's Conclusion That Qualcomm's Use of the Arm Trademarks Creates Any False Understanding of Affiliation, Sponsorship, or Certification as to Source Is Unsupported

77.   The Dhar Report claims that Qualcomm's purportedly unauthorized use of the Arm Trademarks falsely conveys affiliation, sponsorship, or certification as to source.[119] Yet, it fails to provide any valid scientific evidence that sophisticated and specialized purchasers of Qualcomm products would interpret the terms "Arm-based" and "Arm-compliant" as the Dhar Report appears to conclude that they would. Further, the Dhar Report disregards that Qualcomm's purported use of the Arm Trademarks simply identifies technical aspects of its products and that, in the complex tech industry, it is common for companies to articulate the connections between various product components, even in cases where there exists no formal business affiliation among the producers of said components. Finally, the

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[119]   Dhar Report, ¶ 136 ("Qualcomm's unauthorized use of the Arm Trademarks, in particular phrases such as 'Arm-based' and 'Arm compliant,' falsely signifies that the Nuvia Products have been connection [sic] as to source, affiliation, sponsorship, or approval from Arm and have been verified and validated by Arm and that the Nuvia Products are covered by an applicable license to Arm Technology.").

Dhar Report provides quotes from certain news articles without any support that its interpretation of those quotes is aligned with how a relevant audience would interpret them, and without establishing that sophisticated industrial procurement departments would rely on these or similar sources for their purchase decisions. As such, the Dhar Report's conclusion that Qualcomm's use of the Arm Trademarks creates false understanding of affiliation, sponsorship, or certification as to source is unfounded.

78.   The Dhar Report maintains, without basis, that "Qualcomm's unauthorized use of the Arm Trademarks, in particular phrases such as 'Arm-based' and 'Arm compliant,' falsely signifies that the Nuvia Products have been connection [sic] as to source, affiliation, sponsorship, or approval from Arm and have been verified and validated by Arm and that the Nuvia Products are covered by an applicable license to Arm Technology."[120]

79.   Yet, the materials that I have reviewed, including Arm's Branding Guidelines and Arm's Trademark Use Guidelines, do not suggest that written authorization,[121] contact with Arm's

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[120]   Dhar Report, ¶ 136.

[121]   Arm's Trademark Use Guidelines instruct third parties to seek written authorization from Arm's trademarks team for use of the Arm logo and copyright materials, but do not include an analogous instruction for what it calls "referential use" of the Arm word mark. The Dhar Report does not consider the Arm's Trademark Use Guidelines. *See* QCARM_7517739–744 at 739, 741-742.

trademarks team,[122] or any "approval" or having been "verified and validated"[123] by Arm is required for what Arm itself defines as "referential use" of the Arm Trademarks.[124]

80.   Moreover, the Dhar Report offers no empirical analysis to determine whether Qualcomm's use of terms such as "Arm-based" or "Arm-compliant" generally connotes any affiliation, sponsorship, approval, validation, or otherwise certification by Arm. Instead, the Dhar Report relies merely on deposition testimony from two individuals — Will Abbey, Arm's Executive VP and Chief Commercial Officer, ███████████████████ — to conclude that "[t]erms such as 'Arm-based' and 'Arm-compliant' have a particular meaning within the relevant market, which conveys endorsement and sign-off by Arm of such products," and that "these terms/phrases convey to industry participants that a CPU has been verified and validated by Arm according to the process specified in an applicable license agreement."[125]

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[122]   Jonathan Armstrong, Arm's Head of Brand and Creative Services, ████████████
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[123]   Dhar Report, ¶ 136.

[124]   Arm itself puts forward the use of the term "Arm-based" as appropriate in these circumstances. *See* QCARM_7517739–744 at 741-742. Similarly, in deposition testimony that Dr. Dhar relies on to support his claim that "Companies will negotiation the use of these terms [e.g., "Arm-based"] with Arm," Jonathan Armstrong states that Arm "will, you know, have review and discuss and understand exactly what the use of – or why they need to use the brand or the logo or why they're even referencing Arm-based if they don't have a license." This type of *internal* discussion within Arm suggests a reaction to third parties having followed the "referential use" guidelines in Arm's Trademark Use Guidelines, and not a statement about discussions with third parties *prior to* use of a term such as "Arm-based." *See* Dhar Report, ¶ 55, citing Armstrong Deposition, p. 78:10-18.

[125]   Dhar Report, ¶ 117.

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81. Dr. Dhar's reliance on this testimony is misplaced. ███████████████████

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██ Similarly, Mr.

Abbey testified that "[t]he definition *in [his] mind* (emphasis added) of compatibility is that

it passes the verification suite."[126] The Dhar Report offers no evidence, empirical or

otherwise, that purchasers of Qualcomm's products would hold the same or similar belief

regarding the definition of "compatibility" with respect to CPU architecture as Arm's Chief

Commercial Officer, and consequently the Dhar Report offers no basis to assume they

would.

82. The Dhar Report also misleadingly quotes ███████████████████

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[126] Abbey Deposition, p. 84:8-25 ("████████████████████████████████

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[127] Dhar Report, ¶ 113.

[128] ████████████████████████

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83.   In a complex, technical environment, such as the PC or mobile device marketplace, where many different components are compiled to make a final product work, it is a common practice to specify if and how different components are compatible. Since components offered by different companies within a single final product have to be able to interoperate, companies need to provide ways of describing how those components relate to each other, even where there may be no formal business relationship between the component producers. For example, Microsoft states in its publicly available Trademark and Brand Guidelines that third-party app developers (who may program their apps to work with Microsoft's various offerings) must keep "everything about [their] app […] free of Microsoft's Brand Assets. The only exception is that [they] may truthfully state whether [their] app is compatible or interoperable with a Microsoft product or service within the text description [of their] app."[129]

84.   Arm's own publicly available Trademark Use Guidelines[130] recognizes that third parties may need to refer to its technologies, as it explicitly instructs third parties to describe their products as "Arm-based" in order to accurately describe the relationship between the third-party technology and Arm's technologies. In the "Referential use of Arm's trademarks" section of its Trademark Use Guidelines, Arm instructs third parties that they "may refer

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[129]   "Microsoft Trademark and Brand Guidelines," *Microsoft*, available at https://www.microsoft.com/en-us/legal/intellectualproperty/trademarks, accessed on February 12, 2024.

[130]   I note that the Dhar Report refers to Arm's Branding Guidelines, which apply only to holders of valid Arm trademark licenses, as both Branding Guidelines and Trademark Guidelines, without recognizing that Arm makes separate, publicly available Trademark Use Guidelines for non-licensee third parties. *See* Dhar Report, ¶¶ 51-52; ARM_01425245–252; QCARM_7517739–744. Therefore, any opinions offered in the Dhar Report based on the license-holder-relevant Branding Guidelines that speak to what Qualcomm should or should not have done with respect to Arm Trademarks while it did not hold an Arm license are unsupported.

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to Arm-based products by using the word '-based' between the relevant Arm trademark and the relevant third party product" and "may also indicate the relationship of [their] products and services to Arm's products and services using accurate referential phrases."[131] These instructions thus provide a rubric that third parties, such as Qualcomm, can use to refer to Arm's products and services in describing their own products and services without (falsely) signifying affiliation or approval between them.

85.   In this case, third parties may need to describe their products or services as being compatible with Arm's technologies. For example, software designers refer to their technology written to interoperate on Arm technologies as "Arm-based."[132] In fact, ███

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███████   As Arm itself put it in its registration statement, the CPU instruction set is

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[131]   QCARM_7517739–744 at 741-742.

[132]   *See* Deposition of Simon Segars, *Arm Ltd. v. Qualcomm Inc., Qualcomm Technologies, Inc., and NuVia, Inc.,* C.A. No. 22-1146 (MN), United States District Court for the District of Delaware, November 16, 2023, pp. 39:25-40:6 ("████████████████████████████████████

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"essentially a common language for software developers to use."[134] In order to build a product, software developers must know what language they're speaking. Only by knowing which ISA a given piece of technology relies upon can developers reach into the "large library of compatible software which runs on those CPUs."[135] ███████████████

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████████████████████████████████ Moreover, Arm's own corporate deponent, Jonathan Armstrong, Arm's Head of Brand and Creative Services, testified in his deposition that he was not aware of any instance in which Arm had ever taken legal action based on third-party software designers that describe their software as "Arm-based."[136]

86. The Dhar Report cites to some industry articles and states, "industry press covering the technology at issue has used Arm's brand to suggest endorsement, affiliation, or certification of the technology at issue by Arm."[137] The Dhar Report does not provide any explanation or evidence that the audience of those news articles would interpret them as

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[134] ARM_01259705–01015 at 9713 ("Every CPU has an ISA, which defines the software instructions that can be executed by the CPU, essentially a common language for software developers to use.").

[135] ARM_01259705–01015 at 9825 ("The ISA sets the foundation for the large library of compatible software which runs on those CPUs.").

[136] Armstrong Deposition, pp. 80:20-81:23 ████████████████████████████
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█████████████████████ " Objection omitted.").

[137] Dhar Report, ¶ 119.

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suggesting "endorsement, affiliation, or certification" of the at-issue technology by Arm as the Dhar Report claims. Moreover, the cited articles, describing Qualcomm's technology as Arm-based, appear to be focused toward a general readership for a technology-oriented audience. While the news articles might discuss certain technical information, the Dhar Report provides no basis for inferring (as it appears to do) that sophisticated industrial purchasers of Qualcomm's products would rely entirely or in part on these news articles, rather than the technical specifications of the products, to make judgments about affiliation or sponsorship of Qualcomm's products.

87.   As previously stated in **Section V.B**, well-informed, specialist purchasers of Qualcomm's products could be likely to view the term "Arm-based" as an indicator of the technical attributes of the chip, rather than any type of indicator of source. Though the Dhar Report contends the opposite to be true, it provides no evidence — including any surveys, interviews, or other data — to support its position. Moreover, the Dhar Report disregards the fact that industrial procurement departments are capable of testing the technical specifications of the parts that they consider purchasing, and therefore are highly unlikely to be confused regarding the attributes of the product when the performance or attributes of a chip they consider purchasing can be empirically verified.[138] To the extent that any of the few journalists (and one blogger) to which the Dhar Report cites used the term "Arm-based" to refer to the technical capabilities of Qualcomm's products and not to identify sponsorship by Arm, the Dhar Report's conclusion that "participants throughout the

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relevant industry are associating the Nuvia Products with Arm sponsorship"[139] would be incorrect. The Dhar Report does not present any scientific research necessary to support its conclusion that Qualcomm's purported use of the Arm Trademarks have led to any costumer confusion, and as a result, the opinions offered therein are entirely unreliable.

D. The Dhar Report Presents No Evidence of Actual Confusion and Ignores Contradictions by Arm's Own Admissions

88.   Not only has Dr. Dhar not conducted any research to support his conclusion that Qualcomm's purported use of the Arm Trademarks was likely to cause confusion among its customers, the Dhar Report also presents no evidence of *actual* confusion in any market — let alone the relevant B2B market discussed in **Section V.B**.

89.   The Dhar Report both fails to cite, and is inconsistent with, the significant number of statements by Arm itself disclaiming knowledge or awareness of any actual customer confusion. For example, Arm has admitted that it is "not currently aware of any confusion, mistake, or deception related to Qualcomm's use of ARM trademarks in connection with products originally developed under the Nuvia ALA[.]"[140] Similarly, Arm has admitted that "it is not currently aware of instances where a customer has expressed to Arm its confusion, mistake, or deception due to Qualcomm's use of Arm trademarks in connection with products originally developed under the Nuvia ALA."[141]

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[139]   Dhar Report, ¶ 120.

[140]   Arm Ltd.'s Objections and Responses to Qualcomm's Fourth Set of Interrogatories (Nos. 21-25), *Arm Ltd. v. Qualcomm Inc., Qualcomm Technologies, Inc.*, and *NuVia, Inc.*, C.A. No. 22-1146-MN, United States District Court for the District of Delaware, November 17, 2023 ("Fourth Set of Interrogatories"), pp. 18-19.

[141]   Plaintiff Arm Ltd.'s Responses and Objections to Qualcomm's First Requests for Admissions to Plaintiff (Nos. 1-30), *Arm Ltd. v. Qualcomm Inc., Qualcomm Technologies, Inc.*, and *NuVia, Inc.*, C.A. No. 22-1146-MN, United States District Court for the District of Delaware, November 17, 2023 ("First Requests for Admissions to Plaintiff"), p. 14.

90. Moreover, Arm's own corporate deponent, Jonathan Armstrong, Head of Brand Creative

Services, stated several times in deposition that Arm did not have any knowledge of

confusion among its customers, nor that it had taken any steps to remedy any perceived

confusion. Mr. Armstrong testified that he did not know of *any* Arm customers who have

been confused by Qualcomm's use of the Arm Trademarks in relation to Qualcomm's

custom cores, and that Arm has no facts to suggest that any of its customers or Arm's

customers have been confused by Qualcomm's press releases.[142] Armstrong further

testified that he was unaware of any factual basis for believing that Qualcomm's blog posts

using the phrase "Windows on Arm PCs powered by Snapdragon compute platforms" has

given rise to any confusion concerning Arm Trademarks in connection with any Qualcomm

product, nor has Arm contacted Qualcomm to ask it to remove this blog post since its

publication in January 2022.[143] Armstrong also testified that, although he would have been

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[142] Armstrong Deposition, pp. 109:15-110:13 ("

" Objection omitted.).

[143] Armstrong Deposition, pp. 99:1-101:7 ("

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notified in his role "[i]f something was going on outside of [a licensee's] agreement and what was agreed with regards to a usage of those [Arm] marks," he received no such notification "that Qualcomm had any use of the Arm logo or Arm word trademark that fell outside of the agreement and what was agreed with regards to a usage of Arm's trademarks."[144] Finally, Armstrong also testified that he was unaware of any instance, outside of the allegations of this lawsuit, in which Arm ever contacted Qualcomm to ask it to correct or remove a publicly available description of a Qualcomm custom core as "Arm-compatible," "Arm-compliant," or "Arm-based."[145]

91. The Dhar Report's opinions that customers are being confused, or are highly likely to be confused, are unsupported by any evidence, empirical or otherwise, and cannot be relied upon.

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[144] Armstrong Deposition, pp. 58:4-59:6 ("█████████████████████████████████████

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██Objection omitted.").

[145] Armstrong Deposition, p. 104:4-18 ("████████████████████████████████████

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VI. THE DHAR REPORT'S CONCLUSIONS ON HARM TO THE ARM BRAND ARE SPECULATIVE AND DO NOT EXPLAIN THE MECHANISM BY WHICH HARM WOULD OCCUR

92. The Dhar Report makes speculative, forward-looking, and unsupported statements on purported harm from Qualcomm's purportedly unauthorized use of the Arm Trademarks. In particular, the Dhar Report makes generic statements about harm to the Arm brand,[146] diversion of sales from authorized users of Arm Trademarks,[147] and loss of benefits by Nuvia's customers.[148] These statements are based on speculative theory and are untethered to the facts put forward in this matter. Moreover, the Dhar Report does not discuss in concrete detail how the purported harm would arise in the relevant market. To the extent the Dhar Report does articulate any theory of harm, the theories are unsupported and speculative.

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[146] Dhar Report, ¶¶ 127-128 ("Qualcomm's unlicensed use of Arm's Trademarks will cause harm to Arm by resulting in a loss of control to Arm of its brand and goodwill. In general, the loss of brand image and goodwill occurs because any dissatisfaction or problems associated with the infringing user, or its products are likely to be erroneously attributed also to the trademark owner and/or its products. Negative attributions and inferences concerning the infringing user, or its products can also spillover to Arm if it is seen as being associated with such products. […] Qualcomm's unauthorized use of Arm's Trademarks means that how customers view the Arm Mark is now connected to the quality and outcomes associated with the Nuvia Products.").

[147] Dhar Report, ¶ 132 ("Qualcomm's unauthorized use of Arm's Trademark in connection with the Nuvia Products will likely divert sales from authorized users of Arm's Trademark (e.g., Arm's customers whose products are covered by a valid license with Arm).").

[148] Dhar Report, ¶ 133 ("Customers of Nuvia Products themselves would be harmed by the deceptive nature of the sale and the loss of benefits they sought from using Arm's products.").

A. The Dhar Report's Conclusion About Harm to the Arm Brand's Image and Goodwill Is Speculative and Unsupported

93.   The Dhar Report contends that "Qualcomm's unlicensed use of Arm's Trademarks will cause harm to Arm by resulting in a loss of control to Arm of its brand and goodwill."[149] However, beyond such generic statements that merely explain the general concept of loss of brand image and goodwill, the Dhar Report does not precisely define or otherwise specify what that harm is and how that harm would occur in this specific context. Moreover, the Dhar Report does not provide valid evidence for this assertion and ignores evidence in this litigation that actually suggests the opposite, that the Arm brand has not been and is unlikely to be harmed.

94.   The Dhar Report states that "[i]n general, the loss of brand image and goodwill occurs because any dissatisfaction or problems associated with the infringing user, or its products are likely to be erroneously attributed also to the trademark owner and/or its products. Negative attributions and inferences concerning the infringing user, or its products can also spillover to Arm if it is seen as being associated with such products."[150] As with its analysis of customer confusion, the Dhar Report does not specify who would attribute these problems to Arm, nor who would associate Arm with Nuvia's products in this case. Nor does the Dhar Report offer evidence that there would be such "[n]egative attributions and inferences" spilling over to Arm.[151]

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[149]   Dhar Report, ¶ 127.

[150]   Dhar Report, ¶ 127.

[151]   Dhar Report, ¶ 127.

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95. In fact, the Dhar Report has not put forward *any* empirical evidence to suggest that there would be an effect on the goodwill or brand image of the Arm brand as a result of the purported, at-issue trademark infringement.[152] The only evidence the Dhar Report cites in support of its assertion that harm is likely is deposition testimony from Will Abbey, Arm's Executive VP and Chief Commercial Officer, who is not a neutral party. Mr. Abbey testified to his *belief* that "a partner that continues to use Arm confidential information without a contract is – damages our brand and damages our reputation,"[153] but did not provide any support for his testimony.[154]

96. Critically, the Dhar Report ignores evidence in the record contrary to his conclusion, including deposition testimony from Arm's own witnesses stating that they were unaware of any actual harm to Arm, including from loss of goodwill or purported consumer confusion in connection with Arm Trademarks. For example:

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[152] Moreover, a form of empirical analysis employing survey evidence is "virtually demand[ed]" in cases alleging violations of the Lanham Act. *See* Diamond, Shari S., "Reference Guide on Survey Research," in *Reference Manual on Scientific Evidence*, Third Edition, National Academies Press, 2011, pp. 359-423 ("Diamond (2011)"), p. 366 ("A routine use of surveys in federal courts occurs in Lanham Act cases, when the plaintiff alleges trademark infringement or claims that false advertising has confused or deceived consumers. **The pivotal legal question in such cases virtually demands survey research because it centers on consumer perception and memory[.**]" (emphasis added)). *See also* Diamond (2011), pp. 364-365 ("The inquiry under Rule 703 focuses on whether facts or data are 'of a type reasonably relied upon by experts in the particular field in forming opinions or inferences upon the subject.' … Because the survey method provides an economical and systematic way to gather information and draw inferences about a large number of individuals or other units, surveys are used widely in business, government, and, increasingly, administrative settings and judicial proceedings.").

[153] Abbey Deposition, p. 324:2-8 ("███.").

[154] Additionally, I understand that there is a dispute in the case as to whether Qualcomm is using Arm confidential information without a contract, and that Qualcomm's position is that it is not.

a. Mr. Abbey's testimony is directly contradicted by that of Jonathan Armstrong, Arm's Head of Brand and Creative Services, who testified in his capacity as corporate designee that he was not aware of any Arm partners or customers telling Arm that they value Arm Trademarks differently as a result of Qualcomm's use of Arm's word mark, nor was he aware of any Arm customers or licensees taking the view that they do not need to follow Arm Trademark Use Guidelines or Branding Guidelines because of Qualcomm's actions in connection with this lawsuit.[155]

b. Moreover, Mr. Abbey himself testified that (1) Arm customers have not expressed an intent to terminate their TLAs with Arm to use Qualcomm-produced products, (2) none of Arm's customers have breached their contracts with Arm, and (3) Arm has not lost any contracts as a result of the acquisition of Nuvia.[156]

c. Additionally, Arm has admitted that "it is not currently aware of instances since the filing of the Complaint where an ARM licensee or partner has breached its license agreements with ARM citing Qualcomm's alleged breach of Qualcomm's license agreements with ARM."[157]

d. Arm also admitted "that it is not currently aware of instances where a customer or partner has asserted that Qualcomm's use of ARM trademarks in connection with

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[155] Armstrong Deposition, p. 118:11-23 ███

[156] Abbey Deposition, pp. 365:17-367:17.

[157] First Requests for Admissions to Plaintiff, p. 15.

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products previously under development pursuant to the Nuvia ALA damaged ARM's reputation."[158]

  e. Finally, Arm's CEO also testified that Arm has not suffered *any* "concrete harm."[159]

97. Consequently, the only evidence that the Dhar Report provides in support of purported harm to Arm (i.e., a citation from Mr. Abbey) is contradicted by further testimony from the same and other Arm witnesses, as well as by Arm's own admissions in this litigation. As such, the Dhar Report's one piece of evidence on its theory of harm is unreliable and leaves the theory largely unsupported.

98. The Dhar Report further states "Qualcomm's unauthorized use of Arm's Trademarks means that how customers view the Arm Mark is now connected to the quality and outcomes associated with the Nuvia products,"[160] and that any potential negative customer experience with the Nuvia Products could "place Arm's valuable brand asset at risk."[161] This assertion is also speculative, forward-looking, and unsupported. The Dhar Report fails to analyze or describe whether and how the purported negative product features that Nuvia customers may experience would be attributed to Arm. This is a major shortcoming in the Dhar Report because this purported attribution occurs within a technologically sophisticated business-to-business customer base as discussed in **Section V.B**.

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[158] First Requests for Admissions to Plaintiff, p. 16.

[159] Deposition of Rene Haas, *Arm Ltd. v. Qualcomm Inc., Qualcomm Technologies, Inc., and NuVia, Inc.,* C.A. No. 22-1146 (MN), United States District Court for the District of Delaware, December 12, 2023 ("Haas Deposition"), pp. 165:24-166:5 (█████████████████████████████ ███ .").

[160] Dhar Report, ¶ 128.

[161] Dhar Report, ¶ 128.

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99.   Notably, the Dhar Report fails to point to any evidence that such negative experiences with

Qualcomm products have occurred or are likely to occur. Specifically, the Dhar Report

fails to consider that, in contrast with his conclusion, deposition testimony from Qualcomm

witnesses and PC-industry reporting indicate a perception that Qualcomm's custom cores

actually performed *better* than Arm-built cores and were likely to be perceived as higher

performance products by Qualcomm's and/or Arm's customers. For instance:

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g. Further, October 2023 industry reporting from Qualcomm's Snapdragon Summit suggested that Qualcomm's newly unveiled "Snapdragon X Elite platform built on the [Nuvia-based] Oryon processor… easily beat[] the Apple MacBook Pro 13" with an M2 processor and Razer's Blade 15 (2023)" in a benchmarking session conducted for reporters.[168] Another reporter at *Windows Central* noted that "[p]ound-for-pound, the

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[168] Rubino, Daniel, "Qualcomm Brings Receipts: Snapdragon X Elite Gets Benchmarked, Completely Dunks on Apple's M2 Processor," *Windows Central*, October 30, 2023, available at

Snapdragon X platform powered by the Qualcomm Oryon CPU can take on and beat

Apple's M series chips at its own game."[169]

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https://www.windowscentral.com/hardware/laptops/qualcomm-brings-the-receipts-snapdragon-x-elite-gets-benchmarked-proves-it-beats-apples-m2-processor. █████████████████████████

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██████. *See also* Deposition of Paul Williamson, *Arm Ltd. v. Qualcomm Inc., Qualcomm Technologies, Inc., and NuVia, Inc.,* C.A. No. 22-1146 (MN), United States District Court for the District of Delaware, November 9, 2023, p. 220:4-8 ("█████████████████████████████████

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[169] Devine, Richard, "Windows Finally Has Its Apple Mac Moment, and I'm More Excited About the Future of Laptops Than Ever Before," *Windows Central*, October 25, 2023, available at https://www.windowscentral.com/hardware/laptops/windows-has-its-mac-moment-more-excited-about-the-future-of-laptops-than-ever.

[170] █████████████████████████████. *See also* Moorhead, Patrick, "Research Note: Arm's ████████ CPU Is An Audacious Plan To Have The Best Smartphone CPU Core This Year," *Moor Insights & Strategy*, January 8, 2024, available at https://moorinsightsstrategy.com/research-notes/research-note-arms-████████-cpu-is-an-audacious-plan-to-have-the-best-smartphone-cpu-core-this-year/ ("████████' is Arm's next-generation Cortex-X processor, which Arm plans to enable in smartphones shipping at the end of 2024. […] I am told that this is part of Arm CEO Rene Haas's strategy to 'eliminate the performance gap between Arm-designed processors and custom Arm implementations.' This is a big and bold claim because it is so difficult, and Apple has run the table for so long. […] While Arm holds the ISA cards, winning the CPU wars falls on the backs of architects and its developers, who, to this point,

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100.   The Dhar Report fails to offer any coherent or supported explanation of harm to the Arm brand as a result of Qualcomm's purportedly infringing use of the Arm Trademarks. Other than generic statements about Arm's loss of control over its brand image and goodwill, the Dhar Report does not clarify how that image could be affected by Qualcomm's use of the Arm Trademarks in the relevant sophisticated B2B market. In addition to failing to provide concrete support for its generic statements, the Dhar Report also fails to consider relevant evidence that suggests such harm is unlikely to happen in the context of this litigation.

    B.   **The Dhar Report's Claim About Purported Harm to Arm Through Diversion of Sales Is Overly Simplistic, Speculative, and Unsupported**

101.   The Dhar Report states that "Qualcomm's unauthorized use of Arm's Trademark in connection with the Nuvia Products will likely divert sales from authorized users of Arm's Trademark (e.g., Arm's customers whose products are covered by a valid license with Arm)[,]" because they "mistakenly understand […] that Qualcomm's Nuvia Products are equivalent to Arm technology, or somehow supported by Arm."[171] However, the Dhar Report does not provide any concrete description of how or evidence of whether customers would develop this "mistaken[] understand[ing]" in the sophisticated B2B market in which Qualcomm and other Arm licensees compete. Further, the Dhar Report also does not

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haven't been able to achieve CPU performance supremacy versus Apple."); Robinson, Dan, "Arm Cooking Up Powerful Cortex-X CPU to Beat iPhone Performance, Says Industry Watcher," *The Register*, January 11, 2024, available at https://www.theregister.com/2024/01/11/arm_cooking_up_powerful_cortexx/ ("Arm has confirmed it is working on a CPU core expected to deliver a jump in performance, thus taking aim at the closing the gap between its own chips and those produced by Apple… This rivalry exists because Apple has designed its own chips that have made the iPhone models pack a performance punch compared with Android devices, which typically run on chips built around Arm's pre-validated core designs.").

[171]   Dhar Report, ¶ 132.

describe or provide evidence for whether or how this "mistaken[] understand[ing]" would itself cause sales to be diverted from authorized users of Arm Trademarks.

102.   The only explanations that the Dhar Report provides for this purported shift are the unsupported theory that customers "may select a Nuvia Product rather than an Arm product or an Arm licensed product, understanding mistakenly that they are interchangeable"[172] and the similarly unsupported claim that "[t]he use of the familiar and trusted Arm brand will enable Qualcomm to communicate that the Nuvia Products are licensed and have been verified and validated by Arm, thereby facilitating acceptance and adoption of such products[.]"[173] These statements are overly simplistic and unsupported by valid evidence, and also fail to consider the sophisticated and informed nature of the B2B purchases as discussed earlier in **Section V.B**. Indeed, the Dhar Report's assessment is perhaps more akin to a simple consumer purchase decision (e.g., a consumer in the general population buying a much simpler product on a supermarket shelf due to claims on the packaging), and is wholly unsupported by any scientific analysis, methodology, or study.

103.   In addition, the Dhar Report's assertion that customers "may select a Nuvia Product rather than an Arm product or an Arm licensed product" because they may mistakenly believe these products are "interchangeable" completely ignores the value that Qualcomm and other Arm licensees add to the final product. Instead, the Dhar Report simply assumes without support that a primary reason customers purchase these products is because of their use of Arm technology. This assumption is baseless especially because Qualcomm and

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[172]   Dhar Report, ¶ 16.

[173]   Dhar Report, ¶ 126.

other Arm licensees are the entities that (1) ultimately make the final product (or have them made by a third-party), and (2) design, produce, and market the product into which the chip is a component.

104.   Despite hypothesizing about potential diversion of sales from Arm licensees to Qualcomm, the Dhar Report fails to provide evidence that such diversion of sales would be likely to actually occur. The Dhar Report's simplistic description of the process through which Arm could be harmed by purported diversion of sales from Arm licensees to Qualcomm is purely speculative, unsupported, and fails to consider the sophistication of the decision-makers in the relevant marketplace, as described in **Section V.B**.

   C. The Dhar Report Offers No Evidence for Its Claim That Nuvia Customers Would Be Harmed as a Result of Qualcomm's Use of Arm Trademarks

105.   The Dhar Report states that "[c]ustomers of Nuvia Products themselves would be harmed by the deceptive nature of the sale and the loss of benefits they sought from using Arm's products."[174] However, the Dhar Report offers no evidence that such deception would occur or even that it is likely to occur. As discussed above in **Section V.B** the Dhar Report ignores the fact that Qualcomm and Nuvia's customers are sophisticated industrial purchasers that make informed purchase decisions and thus ignores the implication that they are likely to be aware of the nature of Qualcomm's custom cores. [175] Finally, the Dhar Report's claim that Nuvia customers would be deceived and harmed by not receiving

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[174]   Dhar Report, ¶ 133.

[175]   *See, e.g.*, Dhar Report, ¶¶ 93-97.

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Arm's "unique benefits" such as the "support and maintenance from Arm engineers" is vague and unsupported by evidence of such deception.[176]

106. First, the Dhar Report fails to establish that potential purchasers of Nuvia products would be deceived about the nature or benefits of the chips they are purchasing, including whether Qualcomm has a license with Arm. The Dhar Report does not cite any actual evidence that any Qualcomm customer has obtained or is likely to obtain a product they would not expect, or that any Qualcomm customer would complain to either Qualcomm or Arm about a Nuvia product they purchase. The Dhar Report also does not offer any empirical evidence that, going forward, Qualcomm customers are likely to be deceived.

107. Second, the Dhar Report again fails to acknowledge the sophisticated nature of Qualcomm's chip purchasers (as discussed in **Section V.B**), which makes these customers highly likely to understand and appreciate the precise benefits they are receiving in connection with a major purchase, such as SOCs that include multiple technologies. Moreover, Arm's litigation with Qualcomm has been covered in the news.[177] The Dhar Report has not provided any support for the idea that Qualcomm's customers in

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[176] Moreover, the Dhar Report offers no evidence that Arm provides "support and maintenance" to *Nuvia* customers. ██

[177] *See*, *e.g.*, Lee, Leonard, "Arm-Qualcomm Lawsuit Could Muddle US Chip Design Leadership," *Bloomberg Law*, June 13, 2023, available at https://news.bloomberglaw.com/us-law-week/arm-qualcomm-lawsuit-could-muddle-us-chip-design-leadership; Leswing, Kif, "Why Arm's Lawsuit Against Qualcomm Is a Big Deal," *CNBC*, September 1, 2022, available at https://www.cnbc.com/2022/09/01/why-arms-lawsuit-against-qualcomm-is-a-big-deal.html; Clark, Mitchell, "Qualcomm's Server and Laptop Ambitions May Be in Trouble," *The Verge*, August 31, 2022, available at https://www.theverge.com/2022/8/31/23331493/arm-qualcomm-nuvia-lawsuit-architecture-license-servers-desktops.

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sophisticated procurement departments would be unaware of Arm's lawsuit or Arm's allegations about the custom cores, and the potential loss to them of potential Arm benefits, if any.

108.   Third, the Dhar Report asserts that "[c]ustomers seeking to use an Arm product who instead receive a Qualcomm product are harmed and deceived by getting a product that is not in fact sponsored by or affiliated with Arm, and does not come with the unique benefits, like the support and maintenance from Arm engineers, that a true partnership with Arm would bring."[178] The Dhar Report does not clarify how "unique benefits, like the support and maintenance from Arm engineers" would accrue to those Qualcomm's customers who the Dhar Report alleges would be deceived. ████████████████████████████

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██ Further, the Dhar Report does not provide any evidence that customers who would purchase Qualcomm products under the assumption that the products are "Arm-based" would therefore have an expectation of receiving this type of customer service from Arm.

109.   The Dhar Report fails to provide any reasonable support for the opinion that Nuvia customers would be harmed by Qualcomm's purported use of Arm Trademarks, overlooks

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[178]   Dhar Report, ¶ 133.

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the complexities of B2B procurement, and makes unclear statements about Arm's "unique benefits" that Nuvia customers seek.

VII.   THE DHAR REPORT'S ANALYSIS OF FAIR USE IS SPECULATIVE AND INCOMPLETE

110.   The Dhar Report states that "to demonstrate fair use, Qualcomm must show (1) that its unauthorized use of the ARM Trademarks is necessary to describe both ARM's product or service and Qualcomm's product or service; (2) that Qualcomm uses only so much of the ARM Trademarks as is necessary to describe ARM's product; and (3) that Qualcomm's conduct or language reflects the true and accurate relationship between Arm's and Qualcomm's products or services."[180] The Dhar Report opines that "Qualcomm's unauthorized use of the Arm Trademarks would not constitute fair use[,]"[181] although it states further that it has "not conducted a full analysis on why Qualcomm's unauthorized use of the Arm Trademarks would not constitute fair use[.]"[182]

111.   The test Dr. Dhar relies on in evaluating fair use appears to be a reference to what I understand to be a three-part test to judge the "fairness" of referential use of trademarks used by courts, which asks (1) whether the use of the plaintiffs' mark is necessary to describe the plaintiff's product or service and the defendant's product or service, (2) whether only so much of the plaintiff's mark is used as is necessary to describe the plaintiff's product or service, and (3) whether the defendant's conduct or language reflects

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[180]   Dhar Report, ¶ 135.

[181]   Dhar Report, ¶ 136.

[182]   Dhar Report, ¶ 137.

the true and accurate relationship between the plaintiff and the defendant's products or services.[183]

112.   Whether a particular use constitutes "fair use" strikes me as a legal question to be evaluated by a court. Nonetheless, I will address the Dhar Report and Dr. Dhar's fair use opinion based on my experience as a marketing professor and not as a substitute for the judgment of the court.

113.   *First*, Dr. Dhar's analysis is incomplete and speculative. In lieu of a "full analysis," the Dhar Report merely relies on its previous unsupported conclusion that "particular phrases such as 'Arm-based' and 'Arm compliant' falsely signif[y] that the Nuvia Products have been connection [sic] as to source, affiliation, sponsorship, or approval from Arm and have been verified and validated by Arm and that the Nuvia Products are covered by an applicable license to Arm Technology."[184] Specifically, the Dhar Report asserts that Qualcomm's use of the Arm Trademarks "would *not* reflect the true and accurate relationship between Arm and Qualcomm's Nuvia-based Products" (emphasis in original) for two reasons: (1) "there is no licensing relationship between Arm and Qualcomm with respect to the Nuvia Products" and (2) "the Nuvia-based Products have not gone through a verification and validation process with Arm's support and maintenance in order to comply with Arm's ISA requirements."[185]

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[183]   "Fair Use of Trademarks (Intended for a Non-Legal Audience)," *International Trademark Association*, December 16, 2020, available at https://www.inta.org/fact-sheets/fair-use-of-trademarks-intended-for-a-non-legal-audience/.

[184]   Dhar Report, ¶ 136.

[185]   Dhar Report, ¶ 136.

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114.   *Second,* As discussed in **Section V.C** above, the Dhar Report consistently overlooks and ignores that Qualcomm uses the Arm Trademarks in connection with its custom cores *referentially* to describe its products' technical attributes. Although the Dhar Report purports to state that Qualcomm has no license with Arm covering the custom cores (which I understand Qualcomm disputes),[186] even if this were the case, the Dhar Report does not explain how this renders any description of the custom cores as "Arm-based," "Arm-compliant," or "Arm-compatible" to be factually inaccurate, nor does the Dhar Report offer any evidence that relevant customers would take away an inaccurate understanding of the relationship between Qualcomm and Arm from these terms.[187]

115.   As noted above, I understand Qualcomm's description to be factually accurate because the statement describes that Qualcomm's cores are compatible with the Arm ISA — a fact I understand is not in dispute. Therefore, because the Dhar Report provides no empirical evidence that Qualcomm's factually accurate statements about its custom cores would cause relevant customers to take away an inaccurate understanding of the relationship between Arm and Qualcomm, it does not demonstrate that Qualcomm's purported use of the Arm Trademark fails the third step of his test.

116.   *Third*, the Dhar Report fails to consider or discuss the two other factors it lists as relevant, including whether Qualcomm's descriptions of its custom cores as "Arm-based," "Arm-

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[186]   I understand that Qualcomm contends that the ALA "is intended to encourage licensees to develop their own CPU core technology with their own innovations, at their own risk and expense and for their own benefit," and that "Qualcomm can, under the ALA, design, manufacture, and distribute Qualcomm's custom ARM-compatible CPU cores." Defendants' Amended Answer, ¶¶ 43, 183.

[187]   ██

compliant," or "Arm-compatible" are necessary to accurately identify the custom cores' technical attributes and whether it uses the Arm mark only to the degree necessary to do that.[188]

117.   As discussed above, I understand that software engineers and others in the industry need to understand the ISA with which the Qualcomm products are compatible in order to determine whether and how other products will work with Qualcomm's.[189] Accordingly, it is necessary to describe Qualcomm cores as "Arm-based," "Arm-compliant," or "Arm-compatible." Arm itself seems to recognize this, given that its own Trademark Use Guidelines acknowledge that third parties may need to refer to the relationship between their products and Arm technologies and further instruct those parties to describe their products as "Arm-based."[190]

118.   Based upon the examples the Dhar Report has offered, it also appears that Qualcomm uses the Arm Trademarks to a minimal degree: as discussed above, the Dhar Report cites to only two examples of public descriptions by Qualcomm about its Nuvia-based custom core technologies that refer to the Arm Trademarks.[191] The Dhar Report offers no other evidence

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[188]   Dhar Report, ¶ 135.

[189]   ██

[190]   QCARM_7517739–744 at 741-742.

[191]   I note the Dhar Report cites three sources relating to Qualcomm's current use of the Arm Trademarks. However, because the first of the three, a Qualcomm press release published on January 3, 2022 stating there is "broad support from ecosystem partners for the PC industry's transition to Arm®-based computing," and that Qualcomm's "acquisition of NUVIA uniquely positions Qualcomm Technologies to drive this industry wide transition," was published prior to the announcement of Qualcomm's first custom core (the Qualcomm Oryon Custom Core), it is therefore more accurately considered a historical use of the Arm Trademark. I further note that the Dhar Report cites a press release that was published *after* the

of marketing or branding of those technologies that makes more expansive use of the Arm Trademarks.

119.   Because the Dhar Report does not factually support its assertions that Qualcomm's purported use of the Arm Trademarks in connection with Qualcomm's custom cores was and is inaccurate, its logic does little more than assume the conclusion.

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Joel H. Steckel

February 27, 2024

January 3, 2022 press release as a *historical* use of the Arm Trademark, which further supports its classification as also an instance of historical use. *See* Dhar Report, ¶¶ 112(a), 111.

APPENDIX A

CURRICULUM VITAE

<div align="center">

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</div>

EDUCATION

UNIVERSITY OF PENNSYLVANIA, THE WHARTON SCHOOL

Doctor of Philosophy Degree (Marketing/Statistics) awarded, May 1982.
Dissertation Title: "A Game Theoretic and Experimental Approach to the Group Choice Phenomenon in Organizational Buying Behavior;" Professor Yoram Wind, advisor.

Master of Arts Degree (Statistics) awarded May 1980.

Master of Business Administration Degree (Management Science) awarded with Distinction, May 1979.

Elected to Beta Gamma Sigma, May 1979.

COLUMBIA UNIVERSITY

Bachelor of Arts (Mathematics) awarded Summa Cum Laude, May 1977.

Elected to Phi Beta Kappa, May 1977.

ACADEMIC POSITIONS

Visiting Scholar, University of Pennsylvania Carey Law School, September 1 2022 – August 2023.

Vice Dean for Doctoral Education, Stern School of Business, New York University, August 2012-August 2021.

Accounting Department, Acting Chairperson, Stern School of Business, August 2016 – August 2019.

Director PhD Programs, Stern School of Business, New York University, May 2007-July 2012.

Marketing Department Chairperson, Stern School of Business, New York University, July 1998-June 2004.

Professor and Associate Professor, Stern School of Business, New York University, January 1989 - present. Taught courses in Business Strategy, Marketing Management, Marketing Research, Corporate Reputation and Branding, Models of Pricing and Promotion, Field Studies in the New Economy, Marketing Engineering, and Analytic Marketing for Management Consulting. Also

<div align="center">A-1</div>

taught Doctoral Seminars in Mathematical Models in Marketing and Behavioral Research Methods.

Visiting Professor, Wharton School, University of Pennsylvania, January 1995 - December 1995. Taught Core Marketing course.

Visiting Professor, Escola de Pós-Graduação em Ciências Económicas e Empresariais, Universidade Católica Portuguesa, May - June 1992, May - June 1993. Taught Industrial Marketing and Marketing Strategy.

Associate Professor and Assistant Professor, Graduate School of Business, Columbia University, July 1981 - December 1988. Taught MBA-level courses in Industrial Marketing, Marketing Planning, and Marketing Research. Taught three Ph.D.-level Marketing Seminars and Applied Multivariate Statistics.

Visiting Associate Professor, School of Organization and Management, Yale University, September - December 1988. Taught graduate course in Marketing Strategy.

Visiting Assistant and Associate Professor, Graduate School of Management, University of California at Los Angeles, July 1984 - June 1985, January - March 1987. Taught Advanced Marketing Management, Marketing Research, and Strategic Marketing Planning.

Assistant Instructor, Department of Statistics, University of Pennsylvania, July 1979 - June 1980. Assisted in undergraduate and MBA-level courses in Statistics. Taught undergraduate course in Calculus.

Teaching Assistant, Department of Mathematics, Columbia University, September 1976 - May 1977. Assisted in courses in Number Theory and Differential Equations.

PROFESSIONAL INTERESTS

Marketing Strategy and Marketing Research. In particular, marketing research methodology, marketing and branding strategies, digital marketing, legal aspects of marketing, and managerial decision making.

PUBLICATIONS

Books

Legal Aspects of Marketing Theory (ed. with J. Gersen), New York: Cambridge University Press, 2023.

Shift Ahead: How the Best Companies Stay Relevant in a Changing World (with A. Adamson), New York: AMACOM, 2018.

Marketing Research (with D. Lehmann and S. Gupta), Boston: Addison-Wesley Longman, 1998.

Analysis for Strategic Marketing (with V. Rao), Boston: Addison-Wesley Longman, 1998.

Highly Confidential – Attorneys' Eyes Only

The New Science of Marketing: State of the Art Tools for Anticipating and Tracking the Market Forces that will Shape Your Company's Future (with V. Rao), Chicago: Irwin Professional Publishers, 1995.

Journal Articles

"Incorporating Uncertainty in Trademark Surveys: Do Respondents Really Know What They Are Talking About?," (with B. Beebe, R. Germano, and C. Sprigman), The Trademark Reporter, Forthcoming.

"Consumer Uncertainty in Trademark Law," (with B. Beebe, R. Germano, and C. Sprigman), Emory Law Journal, Vol. 72, Issue 3, 2023, 487-546.

"Clearing Up Some Confusion about Dilution: A Reply to Hal Poret," The Trademark Reporter, Vol. 112, 2022, 684ff.

"The Science of Proving Trademark Dilution," (with B. Beebe, R. Germano, and C. Sprigman), The Trademark Reporter, Vol. 110, November-December 2019.

"Testing for Trademark Dilution in the Court and Lab," (with B. Beebe, R. Germano, and C. Sprigman), University of Chicago Law Review, Vol 86, May 2019.

"The Future of Marketing Letters," (with P. Golder and S. Jap), Marketing Letters, Vol. 29, No. 3, September, 2017, 1-5.

"Behavioral Reasons for New Product Failure: Does Overconfidence Induce Over-forecasts?" (with D. Markovitch, A/ Michaut-Denizeau, D. Philip, and W. M. Tracy), Journal of Product Innovation Management, Vol. 32, No. 5, September 2015.

"Modeling Credit Card Share of Wallet: Solving the Incomplete Information Problem," (with Y. Chen), Journal of Marketing Research, Vol. 49, No. 5, October 2012.

"The Role of Consumer Surveys in Trademark Infringement: Evidence From the Federal Courts," (with R. Bird), University of Pennsylvania Journal of Business Law, Vol. 14, Issue 4, Summer 2012, 1013-1054.

"Do Initial Stock Price Reactions Provide a Good Measurement Stick for Marketing Strategies? The Case of Major New Product Introductions in the US" (with D. Markovich), European Journal of Marketing, Vol. 46, Iss. 3, 2012, 406-421.

"When Do Purchase Intentions Predict Sales?" (with V. Morwitz and A. Gupta), International Journal of Forecasting, Vol. 23, November 2007, 347-64.

"Dilution through the Looking Glass: A Marketing View of the Trademark Dilution Revision Act of 2005," (with R. Klein and S. Schussheim), The Trademark Reporter, Vol. 96, No. 3, May-June 2006.

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"Using Capital Markets as Market Intelligence: Evidence from the Pharmaceutical Industry," (with D. Markovich and B. Yeung), Management Science, October 2005.

"Marketing Science – Growth and Evolution," (with J. Hauser, G. Allenby, F.H. Murphy, J.S. Raju, and R. Staelin), Marketing Science, Vol. 24, No. 1, Winter 2005.

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"Choice and the Internet: From Clickstream to Research Stream," (with R. Bucklin, J. Lattin, A. Ansari, S. Gupta, D. Bell, E. Coupey, J.D.C. Little, C. Mela, and A. Montgomery), Marketing Letters, Vol. 13, No. 3, Summer 2002.

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"2001: A Marketing Odyssey," (with E. Brody), Vol. 20, No. 4, Marketing Science, Fall 2001.

"Consumer Strategies for Purchasing Assortments within a Single Product Class," (with Jack K.H. Lee), Journal of Retailing, Vol. 75, No. 3, Fall 1999.

"The Max-Min-Min Principle of Product Differentiation," (with A. Ansari and N. Economides), Journal of Regional Science, May 1998.

"Dynamic Influences on Individual Choice Behavior," (with R. Meyer, T. Erdem, F. Feinberg, I. Gilboa, W. Hutchinson, A. Krishna, S. Lippman, C. Mela, A. Pazgal, and D. Prelic), Marketing Letters, Vol. 8, No. 3, July 1997.

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"Selecting, Evaluating, and Updating Prospects in Direct Mail Marketing," (with V. Rao), Journal of Direct Marketing, Vol. 9, No. 2, Spring 1995.

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"Cross Validating Regression Models in Marketing Research," (with W. Vanhonacker), Marketing Science, Vol. 12, No. 4, Fall 1993.

"Preference Aggregation and Repeat Buying in Households," (with S. Gupta), Marketing Letters, Vol. 4, No. 4, October 1993.

Highly Confidential – Attorneys' Eyes Only

"Roles in the NBA: There's Still Always Room for a Big Man, But His Role Has Changed" (with A. Ghosh), Interfaces, Vol. 23, No. 4, July-August 1993.

"Introduction to `Contributions of Panel and Point of Sale Data to Retailing Theory and Practice'," Journal of Retailing, Vol. 68, No.3, Fall 1992.

"Explanations for Successful and Unsuccessful Marketing Decisions: The Decision Maker's Perspective" (with M.T. Curren and V.S. Folkes), Journal of Marketing, Vol. 56, No. 2, April 1992.

"Locally Rational Decision Making: The Distracting Effect of Information on Managerial Performance" (with R. Glazer and R. Winer), Management Science, Vol. 38, No. 2, February 1992.

"Prospects and Problems in Modeling Group Decisions" (with K.P. Corfman, D.J. Curry, S. Gupta, and J. Shanteau), Marketing Letters, Vol. 2, No. 3, July 1991.

"A Stochastic Multidimensional Scaling Methodology for the Empirical Determination of Convex Indifference Curves in Consumer Preference/Choice Analysis" (with W.S. DeSarbo and K. Jedidi), Psychometrika, Vol. 56, No. 2, June 1991.

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"Longitudinal Patterns of Group Decisions: An Exploratory Analysis" (with K.P. Corfman and D.R. Lehmann), Multivariate Behavioral Research, Vol. 25, No. 3, July 1990.

"Investing in the Stock Market: Statistical Pooling of Individual Preference Judgments," (with N. Capon), Annals of Operations Research, Vol. 23, 1990.

"Judgmental Forecasts of Key Marketing Variables: Rational vs. Adaptive Expectations" (with R. Glazer and R. Winer), International Journal of Forecasting, Vol. 6, No. 3, July 1990.

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"Effective Advertising in Industrial Supplier Directories" (with D.R. Lehmann), <u>Industrial Marketing Management</u>, Vol. 15, No. 2, April 1985.

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"Choice Experiments: Reducing Complexity and Measuring Behavior Rather than Perception" (with R. Fair, K. Shampanier, and A. Cai), in <u>Legal Aspects of Marketing Theory</u> (ed. with J. Gersen), New York: Cambridge University Press, 2023.

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"Dynamic Decision Making in Marketing Channels", with S. Gupta, and A. Banerji), in <u>Experimental Business Research</u>, A. Rapoport and R. Zwick (eds.), Boston, MA: Kluwer Academic Publishers, 2002.

Refereed Proceedings

"PIONEER: Decision Support for Industrial Product Planning" in <u>Efficiency and Effectiveness in Marketing</u>, Proceedings of the American Marketing Association Educator's Conference, Vol. 54, 1988, G.L. Frazier and C.A. Ingene, eds., Chicago.

"Mathematical Approaches to the Study of Power: A Critical Review" in <u>Advances in Consumer Research</u>, Vol. XII, 1985, E. Hirschman and M. Holbrook, eds., Provo, UT.

"On Obtaining Measures from Ranks" in <u>An Assessment of Marketing Thought and Practice</u>, Proceedings of the American Marketing Association Educator's Conference, Vol. 48, B.J. Walker, ed., 1982, Chicago.

Other

"Don Lehmann: My Reflections On A Time Gone By," essay in the Legends of Marketing Series.

"Find the Open Door: A Reflection," in "Reflections of Eminent Marketing Scholars," <u>Foundations and Trends in Marketing</u>, Special Issue, 2022, ed. by Dawn Iacobucci.

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"What Consumers Really Think About Reference Price Labels" (with R. Kirk Fair, K. Shampanier, L. O'Laughlin, and J. Shea), Law 360, March 21, 2017, https://www.analysisgroup.com/globalassets/content/insights/publishing/law360_reference_price_labels.pdf

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"Jerry Wind: A Man Ahead of His Time," essay in the Legends of Marketing Series.

"Is it Worth Anything?: Using Surveys in Intellectual Property Cases?," https://www.analysisgroup.com/Insights/publishing/is-it-worth-anything--using-surveys-in-intellectual-property-cases

"Forecasting Online Shopping," Stern Business, Fall/Winter 2000, pp. 22-27.

"Method to Their Madness," The Industry Standard, August 7, 2000.

Book review of The Application of Regression Analysis by D.R. Wittink, Journal of Marketing Research, Vol. 26, No. 4, November 1989.

Co-author (with many others) of The Statistics Problem Solver, Research and Education Association, New York, 1978.

CONFERENCE PRESENTATIONS

"Innovative Methodologies on Contemporary Trademark Law," (with B. Beebe, R. Germano, and C. Sprigman), CREATe Trade Marks Seminar, University of Glasgow, June 2022.

"Consumer Uncertainty in Trademark Law: An Empirical Investigation," (with B. Beebe, R. Germano, and C. Sprigman), 2021 Intellectual Property Scholars Conference, Cardozo Law School, August 2021.

Highly Confidential – Attorneys' Eyes Only

"Trademark Law's Shallow Empiricism: An Experimental and Theoretical Investigation," (with B. Beebe, R. Germano, and C. Sprigman), Tri State Region IP Workshop, January 2021.

"The Evolving Business Ph.D.," The Third Annual Global PhD Colloquium," Fordham University, April 2019.

"Testing for Trademark Dilution in the Court and Lab," (with B. Beebe, R. Germano, and C. Sprigman), Munich Summer Institute, June 2018.

"Trademark Dilution: Searching for the Elusive Unicorn," Conference on Empirical Legal Studies, Cornell University, October 2017.

"Measuring Trademark Dilution", Conference on Empirical Analysis of Intellectual Property, NYU Law School, October 2014.

"Using Surveys in Intellectual Property Cases: What's the Damage?," AIPLA Spring Meeting, May 2013, Seattle WA.

"Trademark Dilution: An Elusive Concept in the Law," Conference on Brands and Branding in Law, Accounting, and Marketing Kanan Flagler School, University of North Caroline, April 2012

"The Role of Consumer Surveys in Trademark Infringement Cases: Evidence from the Federal Courts," (with R. Bird), AMA Summer Educator's Conference, August 2010, Boston.

"Global Market Share Dynamics: Winners and Losers in a Tumultuous World," (with P. Golder and S. Chang), INFORMS Marketing Science Conference, June 2010, Cologne, Germany.

"Use and Abuse of Consumer Perception Research in Antitrust and Advertising Cases," ABA Antitrust Section Spring Meeting, March 2009, Washington, DC.

"New Product Development: The Stock Market as Crystal Ball," (with D. Markovich), INFORMS Marketing Science Conference, Atlanta, GA., June 2005.

"Modeling Credit Card Usage Behavior: Where is my VISA and Should I Use It?," (with Y. Chen), INFORMS Marketing Science Conference, College Park, Md., June 2003.

"Using Capital Markets as Market Intelligence: Evidence from the Pharmaceutical Industry," (with D. Markovich and B. Yeung), INFORMS Marketing Science Conference, College Park, Md., June 2003.

"Using Capital Markets as Market Intelligence: Evidence from the Pharmaceutical Industry," (with D. Markovich and B. Yeung), Share Price Accuracy and Transition Economies Conference, U. of Mich. Law School, Ann Arbor, Mi., May 2003.

"Modeling Internet Site Visit Behavior," (with E. Bradlow and O. Sak), Joint Statistical Meetings, Indianapolis, August 2000.

"Consumer Strategies for Purchasing Assortments within a Single Product Class," (with Jack K.H. Lee), INFORMS Fall Conference, Philadelphia, November 1999.

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"When Do Purchase Intentions Predict Sales?" (with V. Morwitz and A. Gupta), AMA Advanced Research Techniques Forum, Santa Fe, NM, June 1999.

"Modeling New Product Preannouncements as a Signaling Game," (with H. Jung), University of Mainz Conference on Competition in Marketing, Germany, June 1999.

"A Multiple Idea Point Model: Capturing Multiple Preference Effects from within an Ideal Point Framework," (with J. Lee), Joint Statistical Meetings, Dallas, TX, Aug. 1998.

"Modeling New Product Preannouncements as a Signaling Game," (with H. Jung), INFORMS Marketing Science Conference, Fontainbleau, France, July 1998.

"Dynamic Decision-Making in Marketing Channels: Traditional Systems, Quick Response, and POS Information," (with S. Gupta and A. Banerji), NYU Conference on Managerial Cognition, May 1998.

"When Do Purchase Intentions Predict Sales?" (with V. Morwitz and A. Gupta), INFORMS International Meetings, Barcelona, July 1997.

"Mental Models in Competitive Decision Making: A Blessing and A Curse," Conference on Competitive Decision Making, Charleston, SC, June 1997.

"When Do Purchase Intentions Predict Sales?" (with V. Morwitz and A. Gupta), INFORMS Marketing Science Conference, Berkeley, March 1997.

"Model Adequacy versus Model Comparison: Is the 'Best' Model Any 'Good'?, " (with A. Ansari and P. Manchanda), INFORMS Marketing Science Conference, Berkeley, March 1997.

"Dynamic Decision-Making in Marketing Channels: Traditional Systems, Quick Response, and POS Information," (with S. Gupta and A. Banerji), First Conference in Retailing and Service Sciences, Banff, 1994.

"Dynamic Decision-Making in Marketing Channels: Traditional Systems, Quick Response, and POS Information," (with S. Gupta and A. Banerji), Behavioral Decision Research in Management Conference, Boston, 1994.

"Modeling Consideration Set Formation: The Role of Uncertainty," (with B. Buchanan and S. Sen), TIMS Marketing Science Conference, Tucson, 1994.

"A Cross-Cultural Analysis of Price Conjectures to Environmental Changes," (with V. Rao), TIMS Marketing Science Conference, St. Louis, 1993.

"Decision-Making in a Dynamic Distribution Channel Environment," (with S. Gupta and A. Banerji), TIMS Marketing Science Conference, St. Louis, 1993.

"Cross Validating Regression Models in Marketing Research," (with W. Vanhonacker), TIMS Marketing Science Conference, London, 1992.

"The Influence of Stock Price on Marketing Strategy," (with D. Gautschi and D. Sabavala), TIMS Marketing Science Conference, Wilmington, DE, 1991.

"A Polarization Model for Describing Group Preferences" (with V. Rao), ORSA/TIMS National Fall Meetings, Philadelphia, 1990.

"A Polarization Model for Describing Group Preference," (with V. Rao), Behavioral Decision Research in Management Conference, Philadelphia, 1990.

"Conflict Resolution and Repeat Buying" (with S. Gupta), TIMS Marketing Science Conference, Champaign, Ill., 1990.

"Variety Seeking at the Group Level" (with S. Gupta), Association for Consumer Research Fall Meetings, New Orleans, 1989.

"On Using Attraction Models to Allocate Resources in a Competitive Environment," TIMS Marketing Science Conference, Durham, NC, 1989.

"Multidimensional Scaling with Convex Preferences" (with W.S. DeSarbo), ORSA/TIMS National Fall Meetings, St. Louis, 1987.

"A Social Comparison Model for Describing Group Preference Evaluations" (with V. Rao), TIMS Marketing Science Conference, Jouy-en-Josas, France, 1987.

"The Day the Earth Stood Still," Association for Consumer Research Fall Meetings, Toronto, 1986.

"A Friction Model for Describing and Forecasting Price Movements" (with W. DeSarbo, V. Rao, Y. Wind, and R. Colombo), ORSA/TIMS National Fall Meetings, Miami Beach, 1986.

"An Eigenvalue Method for Measuring Consumer Preferences" (with E. Greenleaf and R. Stinerock), TIMS Marketing Science Conference, Dallas, 1986.

"Creating Conjoint Analysis Experimental Designs without Infeasible Stimuli" (with W. DeSarbo and V. Mahajan), TIMS Marketing Science Conference, Dallas, 1986.

"The Mediating Role of Information in Marketing Managers' Decisions" (with R. Glazer and R. Winer), TIMS Marketing Science Conference, Dallas, 1986.

"Incorporating Interdependencies of Utility Functions into Models of Bargaining" (with S. Gupta), ORSA/TIMS National Fall Meetings, Atlanta, 1985.

"The Formation of Key Marketing Variable Expectations" (with R. Glazer and R. Winer), ORSA/TIMS National Fall Meetings, Atlanta, 1985.

"Does the Nash Equilibrium Really Describe Competitive Behavior?: The Case of Cigarette Advertising," TIMS Marketing Science Conference, Nashville, 1985.

"A Heterogeneous Conditional Logit Model of Choice" (with W. Vanhonacker), ORSA/TIMS National Fall Meetings, Dallas, 1984.

"Using a 'Robust' Response Function to Allocate Resources in a Competitive Environment,"
TIMS Marketing Science Conference, Chicago, 1984.

"Longitudinal Models of Group Choice Behavior," (with D. Lehmann and K. Corfman),
ORSA/TIMS National Fall Meetings, Orlando, 1983.

"Considerations of Optimal Design of New Task Industrial Products," ORSA/TIMS National Fall
Meetings, San Diego, 1982.

"Game Theoretic Choice Models in Organizational Buying Behavior," TIMS Special Interest
Conference in Marketing Measurement and Analysis, Philadelphia, 1982.

OTHER RESEARCH IN PROGRESS

Neuroscience Methods of Measuring Trademark Infringement

Incentive Compatibility in Trademark Surveys

Getting Product Disclaimers Noticed

Marketing Research in the Courtroom vs. the Boardroom: What are the Differences and Do They
Matter? (with R. Bird)

The Impact of Trademark Litigation Outcomes on Brand Equity and Marketing Decision Making

Modeling the Tradeoffs between Marketing Research and Flexible Manufacturing.

INVITED SEMINARS

Columbia University	Spring 1991, Summer 1994
Cornell University	Fall 1983, Spring 1989
Georgetown University	Fall 2006
Pennsylvania State University	Fall 1996, Fall 2006
Rutgers University	Spring 1994
Temple University	Fall 1995
University of California, Berkeley	Spring 1990
University of California, Los Angeles	Spring 1985, Spring 1996
University of California, San Diego	Fall 2003
University of Florida	Spring 1992
University of Mainz, Germany	Summer 1998
University of Michigan	Spring 1993
University of Pennsylvania	Spring 1992, Spring 1995, Spring 1998
University of Southern California	Spring 1987
Washington University, St. Louis	Spring 2003

EDITORIAL SERVICE

Editorships

Co-Editor-in-Chief, *Marketing Letters,* July 2010 – March 2017

Guest editor, special section of <u>Marketing Science</u> on the history of marketing science theory and practice, 2001.

Consulting editor in marketing, Addison-Wesley Longman Academic Publishers, Boston, MA, 1993-1999.

Guest editor, special issue of <u>Journal of Retailing</u> on the use of panel and point of sale data, 1992.

Other

Member of Advisory Board (current), <u>Marketing Letters</u>.

Have served on editorial board or as ad-hoc referee for <u>Journal of Marketing</u>, <u>Journal of Marketing Research</u>, <u>Stanford Law Review</u>, <u>Management Science</u>, <u>Marketing Science</u>, <u>Journal of Consumer Research</u>, <u>Journal of Retailing and Consumer Services</u>, <u>Manufacturing and Service Operations Management</u>, <u>Decision Sciences</u>, <u>Journal of Business and Economic Statistics</u>, <u>Journal of Econometrics</u>, <u>Journal of Retailing</u>, <u>Strategic Information Systems</u>, <u>Review of Marketing Science</u>, <u>Corporate Reputation Review</u>, and <u>Journal of Business Research</u>.

SERVICE

Dissertation Committees Chaired

Joseph Pancras (co-chair)	(Marketing - New York University)
Sergio Meza (co-chair)	(Marketing – New York University)
Dmitri Markovich	(Marketing – New York University)
Heonsoo Jung	(Marketing - New York University)
Jack Lee	(Marketing - New York University)
Asim Ansari (co-chair)	(Marketing - New York University)
Shahana Sen (co-chair)	(Marketing - New York University)

Dissertation Committees Served on

Tingting Fan (Marketing – New York University)
Kei-Wei Huang (Information Systems – New York University)
Sherrif Nassir (Marketing – New York University)
Jane Gu (Marketing – New York University)
Orkun Sak (Marketing – University of Pennsylvania)
Atanu Sinha (Marketing - New York University)
Louis Choi (Marketing - Columbia University)
Sunder Narayanan (Marketing - Columbia University)

Carol Rhodes (Ed. Psych. - Columbia University)
Rita Wheat (Marketing - Columbia University)
Robert Stinerock (Marketing - Columbia University)
Bruce Buchanan (Business Economics - Columbia University)
Chen Young Chang (Marketing - University of Pennsylvania)

Other Discipline Related Service

Chairperson, Marketing Committee, INFORMS, January 2006 – June 2010.
Past President, INFORMS Society on Marketing Science, January 2004 – December 2005.
Founding President, INFORMS Society on Marketing Science, January 2003 – December 2003.
President, INFORMS College on Marketing, January 2002 – December 2002.
President Elect, INFORMS College on Marketing, January 2000- December 2001.
Secretary-Treasurer, INFORMS College on Marketing, January 1998-December 1999.
Association of Consumer Research, Annual Program Committee, 1999.
Co-Organizer of 1996 Conference on Consumer Choice and Decision Making, Arden House,
       Harriman, New York, June 1996.
Organized Marketing Sessions at Fall 1989 TIMS/ORSA Joint National Meetings, New York,
       October 1989.

Other University Related Service

Member, NYU Doctoral Affairs Committee, September 2017 – August 2021.

Member, Research Resources Committee, Stern School of Business, September 2009 – August
2021.

Chair, Statistical and Quantitative Reasoning Task Force, Stern School of Business, September
2005 – August 2007.

Member, Specialization Committee, Stern School of Business, September 2004 - ff.

Member, PhD Oversight Committee, Stern School of Business, January 2006 – May 2007.

Member, Executive Committee, Digital Economy Initiative, Stern School of Business, January
2000 – August 2002.

Member, Board of Directors, Center for Information Intensive Organizations, Stern School of
Business, September 1998 – December 1999.

Member of MBA Committee, Stern School of Business, New York University, 1989-December
1998. Committee was responsible for supervising redesign of MBA programs in 1991 and 1995,
Chairman September 1997-August 1998.

Member of Stern MBA Curriculum Review Committee, September 1997-December 1998.
Committee redesigned MBA Core.

Member of Stern School Committee on Improving Consulting Activities, July 1998-December 1998.

Member of Building Committee, Stern School of Business, New York University, 1990-1992.

Member of Research Committee, Stern School of Business, New York University, 1990-1991.

Elected member of Columbia University Senate. Served on Budget Review and Alumni Relations Committees, 1986-1988.

AWARDS

Awarded the J. Parker Bursk Memorial Prize as the outstanding student participating in the Department of Statistics, University of Pennsylvania, 1979.

Dissertation was awarded Honorable Mention in the 1982 American Marketing Association Dissertation Competition.

Dissertation was named Winner of the 1983 Academy of Marketing Science Dissertation Competition.

Invited speaker at the J. Parker Bursk Memorial Prize Luncheon, Department of Statistics, University of Pennsylvania, 1992.

Invited speaker at American Marketing Association Doctoral Consortium, University of Southern California, 1999.

Cited for outstanding editorial support, Fordham University Pricing Center, Sept. 2002.

Named one of the inaugural winners of the Best Reviewer Award for the *Journal of Retailing,* 2003.

Work recognized by West publishing as one of the outstanding 2012 law review articles on Intellectual Property.

Work recognized with the Highly Commended Paper Award at the Literati Network Awards for Excellence 2013.

SELECTED CONSULTING AND OTHER PROFESSIONAL ACTIVITIES

AOL MovieFone, Inc., New York, NY. Performed general consulting on analyzing caller data for telephone movie information service; Consulted as expert in conjunction with damage assessment in legal proceedings.

Citicorp, New York, NY. Built choice model for bank services.   Gave lectures on Marketing Strategy to CitiCards executives.

Highly Confidential – Attorneys' Eyes Only

Directions for Decisions, Inc., New York, NY and Jersey City, NJ. Consulted on segmentation study of sports apparel market, designed and implemented "Construction Test", a concept design decision tool. Performed general consulting on marketing research practice on an ongoing basis.

Federal Trade Commission, Washington, D.C. Served as consultant on branding strategies in antitrust investigation.

J.C. Penney Co., New York, NY. Performed sales-advertising response analysis. Work was done on request for Management Decision Systems, Inc., Weston, MA.

Pfizer Pharmaceuticals, New York, NY. Conducted seminar on conjoint analysis.

SilverBills, Inc., New York, NY. Member board of advisors.

Union Carbide Corporation, Danbury CT. Built econometric model to forecast prices.

Various Expert Witness Engagements.   Clients include Amazon, AT&T, Avon, Brother International, Capri Sun, Dyson, Epson, Hershey's, JP Morgan Chase, Gerber Products, Johnson & Johnson, K-Swiss, Mead Johnson, Merck KGAA, Microsoft, Monster Cable, McDonald's, New Balance, Pelaton, Playtex, PNC Financial, Proctor & Gamble, Roche, Samsung, Seagate, Sergio Garcia, Sharp, TiVo, Under Armour, Wal-Mart, Warnaco, and various plaintiffs in consumer class actions.

MEMBERSHIPS

American Marketing Association

American Statistical Association

Association for Consumer Research

The Institute for Operations Research and Management Science (INFORMS)

Society for Consumer Psychology

American Association for Public Opinion Research

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APPENDIX B
RECENT TESTIMONY

TESTIMONY IN THE LAST FOUR YEARS

<u>Depositions</u>

Mahindra & Mahindra Ltd. and Mahindra Automotive North America v. FCA US LLC, Case No.: 2:18-CV-12645-GAD-SDD, United States District Court (Eastern District of Michigan); In the Matter of Certain Motorized Vehicles and Components Thereof, Investigation No. 337-TA-1132, United States International Trade Commission, Washington D.C.

Susan Wang, Rene Lee and all others similarly situated, v. StubHub, Inc., Superior Court of the State of California for the County of San Francisco (Case No: CGC-18564120).

Match Group, LLC, v. Bumble Trading Inc., Bumble Holding, LTD., Badoo Trading Limited, Magic Lab Co., Worldwide Vision Limited, Badoo Limited, Badoo Software Limited, Badoo Software Limited, and Badoo Technologies Limited, United States District Court for the District of Texas Waco Division, No. 6:18-CV-00080-ADA.

Brian Gozdenovich, on behalf of himself and all others similarly situated v. AARP, Inc., AARP Services, Inc., AARP Insurance Plan, Unitedhealth Group, Inc. and United Healthcare Insurance Company, United States District Court, District of New Jersey, Case No. 2:18-cv-02788-MCA-MAH.

American Dairy Queen Corporation v. W.B. Mason Co., Inc., United States District Court (District of Minnesota), Civ. Act. No. 0:18-cv-00693-SRM-ECW.

Maglula, LTD. v. Amazon.com, Inc., and Amazon.com Services, LLC (United States District Court For the Eastern District of Virginia, Alexandria Division -Civil Action No.: 1:19-cv-01570-LO-IDD.

Capri Sun GMBH v. American Beverage Corporation, United States District Court for the Southern District of New York; 1:19-cv-1422.

Biologics, Inc. D/B/A Biologics by McKesson Corporation v. OptumRx, Inc., AAA Case No. 01-20-0007-3159 (American Arbitration Association).

Tiffany and Company and Tiffany (NJ) LLC v. Costco Wholesale Corporation, United States District Court, Southern District of New York case number 13 Civ. 1041.

Theta, IP, LLC. v. Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc., United States District Court for the Western District of Texas, Waco Division, Civil Action No.: 6:20-cv-00160-ADA.

Eric Fishon and Alicia Pearlman, individually and on behalf of all others similarly situated v. Peloton Interactive, Inc., United States District Court, Southern District of New York, Case No. 1:19-CV-11711-LJL.

Eric Fishon, individually and on behalf of all others similarly situated, v. Premier Nutrition Corporation f/k/a Joint Juice, Inc., Defendant, United States District Court, Northern District of California – San Francisco Division, Case No. 3:16-cv-06980.

Parts ID, LLC (Plaintiff) v. ID Parts LLC, (Defendant), In the United States District Court for the District of Massachusetts, Civil Action No. 1:20-cv-11253.

Zuru LLC and Zuru Inc. (Petitioners), v. Lego Juris A/S (Respondent), United States Patent and Trademark Office Before the Trademark Trial and Appeal Board, Reg. Nos.: 1,018,875 and 2,245,652.

24-7 Bright Star Healthcare, LLC v. Res-Care, Inc. d/b/a BrightSpring Health Services, United States District Court, Northern District of Illinois - Eastern Division, Case No. 1:21-cv-4609.

State of Arizona, *ex rel.* Mark Brnovich, Attorney General, v. Google LLC, Superior Court of the State of Arizona in and for the County of Maricopa, Case No. CV2020-006219.

Adidas America, Inc. and Adidas AG v. Thom Browne Inc., United States District Court, Southern District of New York, Case No. 1:21-CV-05615

Ryan Hardin, et al v. Samsung Electronics Co. Ltd. et al., United States District Court, Eastern District of Texas – Marshall Division, Case No. 2:21-CV-0290-JRG.

U.S. Dominion, Inc., Dominion Voting Systems, Inc., and Dominion Voting Systems Corporation v. Fox News Network, LLC, Superior Court for the State of Delaware, Case No. N21C-03-257 EMD.

State of North Dakota v. United States of America, United States District Court, District of North Dakota – Western Division, Case No. 1:19-cv-150-DMT-ARS.

Chervon (HK) Limited, Chervon North America Inc., v. One World Technologies, Inc., Techtronic Industries Co. Ltd, Homelite Consumer Products, Inc., United States District Court for the District of Delaware, Case No.: 19-1293-LPS-SRF.

Vans. Inc.; and VF Outdoor, LLC v. Walmart, Inc.; The Doll Maker, LLC; Trendy Trading, LLC; and ACI International, United States District Court for the District of Central California, Southern Division, Case No. 8:21-cv-01876-DOC-KES.

Trial

Adidas America, Inc. and Adidas AG v. Thom Browne Inc., United States District Court, Southern District of New York, Case No. 1:21-CV-05615.

Parts ID, LLC (Plaintiff) v. ID Parts LLC, (Defendant), In the United States District Court for the District of Massachusetts, Civil Action No. 1:20-cv-11253.

Arbitration Hearing

Biologics, Inc. D/B/A Biologics by McKesson Corporation v. OptumRx, Inc., AAA Case No. 01-20-0007-3159 (American Arbitration Association).

Preliminary Injunction Hearing

Danone US, LLC. v. Chobani, LLC., Case Action No. 18 CV 11702, United States District Court (Southern District of New York)

Other Hearings

In the Matter of Distribution of the 2010, 2011, 2012, 2013 Cable Royalty Funds, (Before the Copyright Royalty Judges, Washington D.C.) Docket No. 14-CRB-0010-CD (2010-13)

In the Matter of Certain Motorized Vehicles and Components Thereof, Investigation No. 337-TA-1132, United States International Trade Commission, Washington D.C.

APPENDIX C

MATERIALS CONSIDERED

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Court Filings

Arm Ltd.'s Objections and Responses to Qualcomm's Fourth Set of Interrogatories (Nos. 21-25), *Arm Ltd. v. Qualcomm Inc., Qualcomm Technologies, Inc.*, *and NuVia, Inc.,* C.A. No. 22-1146-MN, United States District Court for the District of Delaware, November 17, 2023.

Complaint, *Arm Ltd. v. Qualcomm Inc., Qualcomm Technologies, Inc.*, *and NuVia, Inc.,* Case No.: 1:22-cv-01146-UNA, United States District Court for the District of Delaware, August 31, 2022.

Defendants' Answer and Defenses to Plaintiff's Complaint and Jury Demand and Defendants' Amended Counterclaim, *Arm Ltd. V. Qualcomm Inc., Qualcomm Technologies, Inc., and NuVia, Inc.*, C.A. No. 22-1146 (MN), United States District Court for the District of Delaware, October 26, 2022.

Plaintiff Arm Ltd.'s Responses and Objections to Qualcomm's First Requests for Admissions to Plaintiff (Nos. 1-30), *Arm Ltd. v. Qualcomm Inc., Qualcomm Technologies, Inc.*, *and NuVia, Inc.,* C.A. No. 22-1146-MN, United States District Court for the District of Delaware, November 17, 2023.

Expert Reports

Expert Report of Ravi Dhar, *Moab Industries, LLC. v. Chrysler Group LLC,* C.A. No. 3:12-cv-08247-HRH, United States District Court for the District of Arizona, March 7, 2014.

Expert Report of Ravi Dhar Regarding Trademark Infringement, *Arm Ltd. v. Qualcomm Inc., Qualcomm Technologies, Inc.*, *and NuVia, Inc.,* C.A. No. 22-1146-MN, United States District Court for the District of Delaware, December 20, 2022, and materials considered.

Depositions

Deposition of Christiano Amon, *Arm Ltd. v. Qualcomm Inc., Qualcomm Technologies, Inc.*, *and NuVia, Inc.,* C.A. No. 22-1146-MN, United States District Court for the District of Delaware, November 15, 2023.

Deposition of James Thompson, *Arm Ltd. v. Qualcomm Inc., Qualcomm Technologies, Inc.*, *and NuVia, Inc.,* C.A. No. 22-1146-MN, United States District Court for the District of Delaware, November 28, 2023.

Deposition of Jonathan Armstrong, *Arm Ltd. v. Qualcomm Inc., Qualcomm Technologies, Inc.*, *and NuVia, Inc.,* C.A. No. 22-1146, United States District Court for the District of Delaware, December 8, 2023.

Deposition of Michael Roberts, *Arm Ltd. v. Qualcomm Inc., Qualcomm Technologies, Inc.*, *and NuVia, Inc.,* C.A. No. 22-1146-MN, United States District Court for the District of Delaware, November 28, 2023.

Deposition of Paul Williamson, *Arm Ltd. v. Qualcomm Inc., Qualcomm Technologies, Inc.*, *and NuVia, Inc.,* C.A. No. 22-1146 (MN), United States District Court for the District of Delaware, November 9, 2023.

Deposition of Rene Haas, *Arm Ltd. v. Qualcomm Inc., Qualcomm Technologies, Inc.*, *and NuVia, Inc.,* C.A. No. 22-1146 (MN), United States District Court for the District of Delaware, December 12, 2023.

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Deposition of Simon Segars, *Arm Ltd. v. Qualcomm Inc., Qualcomm Technologies, Inc., and NuVia, Inc.,* C.A. No. 22-1146 (MN), United States District Court for the District of Delaware, November 16, 2023.

Deposition of Will Abbey, *Arm Ltd. v. Qualcomm Inc., Qualcomm Technologies, Inc., and NuVia, Inc.,* C.A. No. 22-1146-MN, United States District Court for the District of Delaware, October 27, 2023.

Deposition of Ziad Asghar, *Arm Ltd. v. Qualcomm Inc., Qualcomm Technologies, Inc., and NuVia, Inc.,* C.A. No. 22-1146-MN, United States District Court for the District of Delaware, November 8, 2023.

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Other

Conversation with Ziad Asghar, February 20, 2024.

EXHIBIT 16

Page 1

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 1              UNITED STATES DISTRICT COURT
 2              FOR THE DISTRICT OF DELAWARE
 3                      ---o0o---
 4
 5
 6
        ARM LTD., a U.K. corporation,    )
 7                                       )
                        Plaintiff,       )
 8                                       )
               vs.                       )  Case No.
 9                                       )  22-1146-MN
        QUALCOMM INC., a Delaware        )
10      corporation, QUALCOMM           )
        TECHNOLOGIES, INC., a Delaware   )
11      corporation, and NUVIA, INC., a  )
        Delaware corporation,            )
12                                       )
                        Defendants.      )
13                                       )
14
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            WEDNESDAY, NOVEMBER 15, 2023
18
            DEPOSITION OF CRISTIANO AMON
19
       HIGHLY CONFIDENTIAL, ATTORNEYS' EYES ONLY
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22
23
24
        REPORTER: BALINDA DUNLAP, CSR 10710, RPR, CRR, RMR
25
```

Page 2

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 1              A P P E A R A N C E S
 2                      ---o0o---
 3   FOR THE PLAINTIFF:
 4          MORRISON & FOERSTER
            425 Market Street
 5          San Francisco, California 94105
            BY: MICHAEL JACOBS, ESQ.
 6          (415) 268-7455
            mjacobs@mofo.com
 7
            MORRISON & FOERSTER
 8          4200 Republic Plaza
            370 Seventeenth Street
 9          Denver, Colorado  80202
            BY: SARAH BRICKEY, ESQ.
10          (303) 592-2204
            sbrickey@mofo.com
11
12   FOR THE DEFENDANTS:
13          PAUL WEISS
            2001 K Street, NW
14          Washington, D.C.  20006-1047
            BY: WILLIAM ISAACSON, ESQ.
15             MELISSA F. ZAPPALA, ESQ.
            (202) 223-7313
16          wisaacson@paulweiss.com
            mzappala@paulweiss.com
17
18   ALSO PRESENT:
19          Peter Matteson, Videographer
            Kurt Kjelland, Qualcomm
20
21
22
23
24
25
```

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INDEX OF EXHIBITS
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INDEX OF EXHIBITS
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1   SAN FRANCISCO, CALIFORNIA, NOVEMBER 15, 2023
2   ---o0o---
3   BE IT REMEMBERED that on Wednesday, the
4   15th day of November 2023, commencing at the hour
5   of 8:08 a.m. thereof, at 535 Mission Street, Suite
6   2400, San Francisco, California, before me, Balinda
7   Dunlap, a Certified Shorthand Reporter in and for
8   the County of San Francisco, State of California,
9   remotely appeared:
10   THE VIDEOGRAPHER: This is the start of
11 media labeled No. 1 of the video-recorded
12 deposition of Cristiano Amon in the matter of ARM
13 Ltd. versus Qualcomm, Inc., et al., in the United
14 States District Court for the District of Delaware,
15 Case No. 22-1146-MN.
16   This deposition is being held at 535
17 Mission Street, 24th Floor, San Francisco,
18 California on November 15th, 2023, at approximately
19 8:08 a.m.
20   My name is Peter Matteson. I am the legal
21 video specialist from Esquire Deposition Solutions,
22 located at One Sansome Street, No. 3500, San
23 Francisco, California 94104. The court reporter is
24 Balinda Dunlap in association with Esquire
25 Deposition Solutions.

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1   Counsel, please introduce yourself.
2   MR. JACOBS: Michael Jacobs, Morrison &
3   Foerster, for the plaintiff. With me is Sarah
4   Brickey.
5   MR. ISAACSON: Bill Isaacson from Paul
6   Weiss for Qualcomm, also Melissa Zappala of Paul
7   Weiss for Qualcomm.
8   MR. KJELLAND: Kurt Kjelland for Qualcomm.
9   THE VIDEOGRAPHER: Thank you. Will the
10 court reporter please swear in the witness.
11   CRISTIANO AMON
12   called as a witness by the Plaintiff,
13 having been sworn to tell the truth, the whole
14 truth, and nothing but the truth, was examined and
15 testified as follows:
16   THE VIDEOGRAPHER: Please proceed.
17   EXAMINATION BY MR. JACOBS
18   Q. Good morning, Mr. Amon.
19   A. Good morning.
20   MR. JACOBS: I printed out your LinkedIn
21 profile. I have marked as Exhibit 1 the LinkedIn
22 profile of Cristiano Amon.
23   (Reporter marked Exhibit No. 1 for
24   identification.)
25   Q. BY MR. JACOBS: Mr. Amon, is this profile

Page 12

1   correct?
2   A. Yes, it is.
3   Q. What is the difference between QCT,
4   Qualcomm Technologies, Inc., and Qualcomm, Inc.?
5   A. Qualcomm Technologies, Inc., it is a
6   wholly-owned subsidiary of Qualcomm that carries
7   our semiconductor business.
8   Q. And QCT is?
9   A. It stands for Qualcomm CDMA Technologies.
10 That's the semiconductor segment of Qualcomm.
11   Q. And then Qualcomm, Inc. is the parent
12 company?
13   A. That is correct.
14   Q. How did your duties change when you
15 assumed the role of president and chief executive
16 officer in July of 2021 as compared with president
17 in the preceding period?
18   A. When I was president, I had the operating
19 responsibility. And as I became CEO, I also had
20 other corporate functions as well.
21   Q. What was your role in the acquisition of
22 ARM?
23   A. We didn't acquire ARM.
24   Q. I'm sorry. What was your role in the
25 acquisition of NuVia?

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1 were very worried. That's where he was asking me,
2 if you're worried, I'm calm. Then I told him I
3 will ship the product to Samsung.
4   Q.   And did anything happen -- sorry. Strike
5 that.

11   (Reporter marked Exhibit No. 47 for
12   identification.)
13   Q.   BY MR. JACOBS: 47. 47 is an email thread
14 that ends with an email to you from Jonathan
15 Weiser. Do you see that?
16   A.   Yes.
17   Q.   Who is Jonathan -- is it Weiser? Yes,
18 Weiser.
19   A.   Jonathan Weiser.
20   Q.   Who is he?
21   A.   He's an attorney at Qualcomm.
22   Q.   And he says, "Alvaro and I had a call with
23 legal this morning." Do you see that?
24   A.   Yes.
25   Q.   And Alvaro, remind me, I think we talked

Page 178

1 about him before. He's in legal also?
2   A.   Alvaro, we talked about that before. He's
3 antitrust.

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3   (Reporter marked Exhibit No. 48 for
4   identification.)

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[REDACTED]

11   Q.   In the second paragraph of this article
12 the writer says "Qualcomm wasn't expected to show
13 the fruits of his NuVia acquisition, revealing
14 earlier this year that the chips are due in late
15 2023. It might be a small thing, but Qualcomm
16 executive said that the Oryon chips would ship in
17 2023, sans" -- I think meaning without -- "the
18 'late' qualifier." Do you see that?
19   A.   Yes, I do.
20   Q.   So this is written in November of 2022,
21 almost a year ago to the day?
22   A.   Correct.
23   Q.   When will -- what's your current best
24 assessment when Oryon chips will ship?
25   A.   Oryon are ready. We achieve CS, which is

Page 182

1   commercial sample. So we're now -- we're now
2   shipping Oryon to customers. They are doing
3   development platforms.

[REDACTED]

14   Q.   You used the phrase "commercial sampling,
15 CS"?
16   A.   Yes.
17   Q.   Is that different from commercial quantity
18 shipment?
19   A.   The way our business works in
20 semiconductors -- I'll give an example on phones.
21 We will finish our product, and our product is
22 finished when we declare CS. CS means commercial
23 samples, which means it's already the commercial
24 hardware, the hardware won't go through any
25 changes.

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1   And we already have the first release of
2   the software. That goes into an OEM that is going
3   to build that into their product. We started
4   shipping in volumes when the OEM product's going to
5   manufacturing.
6   And after they leave the factory, they go
7   into the shelves and get purchased by. Usually
8   there is a time delay. For example -- as an
9   example, [REDACTED]

[REDACTED]

16   A.   Correct. Remember the chipset is one
17 component on another product that has a number of
18 other components with different schedules as well.
19   Q.   What is the -- do you happen to know what
20 the documentation associated with [REDACTED] comprises?
21   A.   In my position, I will not know that level
22 of detail.
23   Q.   Who would know that?
24   A.   I think product managers would know that.
25 The customer engineering dedicated to [REDACTED] would

Page 184

1   know that.
2   Q.   Is there a product manager -- lead product
3   manager for [REDACTED]?
4   A.   There is one.
5   Q.   Who is that?
6   A.   I don't know the name.
7   Q.   Next paragraph. "Qualcomm executives
8   didn't address an unexpected lawsuit by the
9   company's IP provider, ARM Ltd., against Qualcomm
10 earlier this year. That would seem to put
11 Qualcomm's development of its next-gen NuVia/Oryon
12 chips in jeopardy." Do you see that?
13   A.   Yes.
14   Q.   And then you go on -- or then the article
15 goes on. Sorry. "(Officially, Qualcomm regards
16 Oryon as its intellectual property -- 'the creation
17 of our custom CPU was started by NuVia engineers
18 while employed at NuVia and, after the acquisition
19 of NuVia by Qualcomm Technologies, the custom CPU
20 was completed by engineers at Qualcomm
21 Technologies,' a representative told PCWorld after
22 this article was published." Quote -- sorry. "It
23 will be 'implemented in Snapdragon technology.'"
24 Do you see that?
25   A.   Yes.

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1   Q.   The statement by the Qualcomm
2   representative that's reported there, is that
3   statement consistent with your understanding?
4   A.   I think it's -- it's an
5   oversimplification. I will go back to the
6   conversation we had before.
7   Qualcomm had acquired NuVia. We had
8   maintained the IP and intellectual property and
9   design that was created by NuVia independent of
10   ARM, and we had completed the product ourselves for
11   new end market based on Qualcomm IP and the
12   Qualcomm ALA, and that would end up being ▮▮▮
13   ▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮
14   MR. JACOBS: Why don't we just take a few
15   minutes. We can get back here at 1:40, and I'll
16   see if I have any other remaining questions.
17   THE WITNESS: All right. Thank you very
18   much.
19   THE VIDEOGRAPHER: We are off the record
20   at 1:34 p.m.
21   (Whereupon a recess was taken.)
22   THE VIDEOGRAPHER: We are back on the
23   record at 1:44 p.m.
24   Q.   BY MR. JACOBS: Sir, do you have any
25   contingency plan to address the possibility that

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1   Qualcomm loses the litigation with ARM and is
2   barred from shipping products ▮▮▮▮▮▮▮▮▮▮
3   ▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮?
4   MR. ISAACSON: Objection to form.
5   THE WITNESS: I will answer the question
6   in the following manner. In the event that
7   Qualcomm is not able to ship a product for whatever
8   reason, I think what is going to happen is we're
9   going to lose that product cycle.
10   What Qualcomm is most likely going to do,
11   depending on the circumstances, we'll have to
12   redesign the process, and it is going to be two
13   different options.
14   ▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮
15   ▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮
16   ▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮
17   ▮▮▮▮▮▮▮▮▮
18   I think the answer is a product cycle will
19   be missed.
20   MR. JACOBS: No further questions. Thank
21   you, sir.
22   THE WITNESS: All right. Thank you.
23   EXAMINATION BY MR. ISAACSON
24   Q.   I just have one question. If you referred
25   to Qualcomm products with NuVia designs, what do

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1   you mean by "NuVia designs"?
2   A.   It means the NuVia team which is now part
3   of Qualcomm CPU team are working on next generation
4   CPUs for Qualcomm, which is ▮▮▮▮▮▮▮▮▮
5   ▮▮▮▮▮▮▮▮▮.
6   MR. ISAACSON: Nothing else.
7   MR. JACOBS: Nothing further.
8   THE VIDEOGRAPHER: This is the end of this
9   video-recorded deposition of Cristiano Amon on
10   November 15th, 2023. We are off the record at 1:45
11   p.m.
12   (Whereupon the proceedings were
13   concluded at 1:45 p.m.)
14   ---o0o---
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1   I have read the foregoing deposition transcript
2   and by signing hereafter, approve same.
3   Dated_____.
4
5   _____
6   (Signature of Deponent)
7
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Page 189

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 1              DEPOSITION OFFICER'S CERTIFICATE
 2                (Civ. Proc. § 2025.520(e))
 3   STATE OF CALIFORNIA      )
 4                            )    Ss
 5   COUNTY OF SAN FRANCISCO  )
 6          I, BALINDA DUNLAP, CSR #10710, hereby
 7   certify:
 8          I am a duly qualified Certified Shorthand
 9   Reporter, in the State of California, holder of
10   Certificate Number CSR 10710 issued by the Court
11   Reporters Board of California and which is in full
12   force and effect.  (Bus. & Prof. § 8016)
13          I am not financially interested in this
14   action and am not a relative or employee of any
15   attorney of the parties, or of any of the parties.
16   (Civ. Proc. § 2025.320(a))
17          I am authorized to administer oaths or
18   affirmations pursuant to California Code of Civil
19   Procedure, Section 2093(b) and prior to being
20   examined, the deponent was first placed under oath
21   or affirmation by me.  (Civ. Proc. §§ 2025.320,
22   2025.540(a))
23          I am the deposition officer that
24   stenographically recorded the testimony in the
25   foregoing deposition and the foregoing transcript
```

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 1   is a true record of the testimony given.  (Civ.
 2   Proc. § 2025.540(a))
 3          I have not, and shall not, offer or
 4   provide any services or products to any party's
 5   attorney or third party who is financing all or
 6   part of the action without first offering same to
 7   all parties or their attorneys attending the
 8   deposition and making same available at the same
 9   time to all parties or their attorneys.  (Civ.
10   Proc. § 2025.320(b))
11          I shall not provide any service or product
12   consisting of the deposition officer's notations or
13   comments regarding the demeanor of any witness,
14   attorney, or party present at the deposition to any
15   party or any party's attorney or third party who is
16   financing all or part of the action, nor shall I
17   collect any personal identifying information about
18   the witness as a service or product to be provided
19   to any party or third party who is financing all or
20   part of the action.  (Civ. Proc. § 2025.320(c))
21
22   Dated: December 4, 2023
23   _____
24             Balinda Dunlap
25
```

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```
 1           DEPOSITION OFFICER'S CERTIFICATE
              (Civ.Proc. § 2025.520(e))
 2
     STATE OF CALIFORNIA    )
 3                          )  Ss.
     COUNTY OF SAN FRANCISCO )
 4
 5            I, Balinda Dunlap, hereby
 6   certify:
 7          I am the deposition officer that
 8   stenographically recorded the testimony in the
 9   foregoing deposition.
10          Written notice pursuant to Code of Civil
11   Procedure, Section 2025.520(a), having been sent,
12   the deponent took the following action within the
13   allotted period with respect to the transcript of
14   the deposition:
15          (  ) In person, at the office of the
16   deposition officer, made the changes set forth on
17   the original of the transcript.  (The parties
18   attending the deposition have been notified of said
19   changes.)
20          (  ) Approved the transcript by signing
21   it.
22          (  ) Refused to approve the transcript by
23   not signing it.
24          (  ) By means of a signed letter, made the
25   changes and approved or refused to approve the
```

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 1   transcript as set forth therein.  (Said letter has
 2   been attached to the original transcript and copies
 3   thereof mailed to all parties attending the
 4   deposition.)
 5          (  ) Failed to approve the transcript
 6   within the allotted time period.
 7   Dated: December 4, 2023.
 8
 9   _____
10
11   Balinda Dunlap
12
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 1   Reference No.: 10401728
 2
 3   Case:  ARM LTD. V. QUALCOMM INC.
 4
           DECLARATION UNDER PENALTY OF PERJURY
 5
          I declare under penalty of perjury that
 6   I have read the entire transcript of my Depo-
     sition taken in the captioned matter or the
 7   same has been read to me, and the same is
     true and accurate, save and except for
 8   changes and/or corrections, if any, as indi-
     cated by me on the DEPOSITION ERRATA SHEET
 9   hereof, with the understanding that I offer
     these changes as if still under oath.
10
11         _____
12         Cristiano Amon
13
14          NOTARIZATION OF CHANGES
15              (If Required)
16
17   Subscribed and sworn to on the _____ day of
18
19   _____, 20____ before me,
20
21   (Notary Sign)_____
22
23   (Print Name)                   Notary Public,
24
25   in and for the State of _____
```

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```
 1   Reference No.: 10401728
     Case:  ARM LTD. V. QUALCOMM INC.
 2
 3   Page No._____Line No._____Change to:_____
 4   _____
 5   Reason for change:_____
 6   Page No._____Line No._____Change to:_____
 7   _____
 8   Reason for change:_____
 9   Page No._____Line No._____Change to:_____
10   _____
11   Reason for change:_____
12   Page No._____Line No._____Change to:_____
13   _____
14   Reason for change:_____
15   Page No._____Line No._____Change to:_____
16   _____
17   Reason for change:_____
18   Page No._____Line No._____Change to:_____
19   _____
20   Reason for change:_____
21   Page No._____Line No._____Change to:_____
22   _____
23   Reason for change:_____
24
         SIGNATURE:_____DATE:_____
25   Cristiano Amon
```

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 1   Reference No.: 10401728
     Case:  ARM LTD. V. QUALCOMM INC.
 2
 3   Page No._____Line No._____Change to:_____
 4   _____
 5   Reason for change:_____
 6   Page No._____Line No._____Change to:_____
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 8   Reason for change:_____
 9   Page No._____Line No._____Change to:_____
10   _____
11   Reason for change:_____
12   Page No._____Line No._____Change to:_____
13   _____
14   Reason for change:_____
15   Page No._____Line No._____Change to:_____
16   _____
17   Reason for change:_____
18   Page No._____Line No._____Change to:_____
19   _____
20   Reason for change:_____
21   Page No._____Line No._____Change to:_____
22   _____
23   Reason for change:_____
24
         SIGNATURE:_____DATE:_____
25   Cristiano Amon
```

EXHIBIT 17

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Qualcomm Previews Snapdragon X Elite SoC: Oryon CPU Starts in Laptops

84
Comments

by **Ryan Smith** on October 24, 2023 3:00 PM EST

Posted in CPUs   Arm   Qualcomm   Adreno   Laptops   SoCs   NUVIA   Snapdragon X Elite   Oryon

While Qualcomm has become wildly successful in the Arm SoC market for Android smartphones, their efforts to parlay that into success in other markets has eluded them so far. The company has produced several generations of chips for Windows-on-Arm laptops, and while each has incrementally improved on matters, it's not been enough to dislodge a highly dominant Intel. And while the lack of success of Windows-on-Arm is far from solely being Qualcomm's fault – there's a lot to be said for the OS and software – silicon has certainly played a part. To make serious inroads on the market, it's not enough to produce incrementally better chips – Qualcomm needs to make a major leap in performance.

Now, after nearly three years of hard work, Qualcomm is getting ready to do just that. This morning, the company is previewing their upcoming Snapdragon X Elite SoC, their next-generation Arm SoC designed for

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But we're getting ahead of ourselves. For now let's focus on the Snapdragon X Elite SoC and the Oryon cores underpinning it.

How To Choose A CPU

The CPU (central processing unit) is your computer's brain.

While this morning's announcement from Qualcomm is far from a deep dive on the hardware, it's our first look at what will be Qualcomm's flagship SoC, and the new CPU cores within it. With a projected launch date of mid-2024, the first laptops based on the SoC are still several months away from hitting retail shelves – and about a year delayed overall. None the less, Qualcomm has finished their silicon development work, and with the chip's specifications locked down, the company is now on to polishing things for a launch next year.

The Oryon CPU cores within the Snapdragon X Elite are the culmination of Qualcomm's Nuvia acquisition from early 2021, and an even longer period of work for the Nuvia team. The ambition of the team, and the importance of the custom Arm architecture CPU cores, cannot be overstated. So the Snapdragon X Elite is going to be an interesting chip on multiple levels, as it sets the pace for the next generation of Qualcomm chip

AnandTech	Snapdragon X Elite	Snapdragon 8cx Gen 3	Snapdragon 8cx Gen 2	Snapdragon 8cx Gen 1
Prime Cores	12x Oryon 3.80 GHz 2C Turbo: 4.3GHz	4x C-X1 3.00 GHz	4 x C-A76 3.15 GHz	4 x C-A76 2.84 GHz
Efficiency Cores	*N/A*	4x C-A78 2.40 GHz	4 x C-A55 1.80 GHz	4 x C-A55 1.80 GHz
GPU	Adreno SD X Elite 4.6 TFLOPS	Adreno 8cx Gen 3	Adreno 690	Adreno 680
NPU	Hexagon 45 TOPS (INT8)	Hexagon 8cx Gen 3 15 TOPS	Hexagon 690 9 TOPS	Hexagon 690 9 TOPS
Memory	8 x 16-bit LPDDR5x-8533 136GB/sec	8 x 16-bit LPDDR4x-4266 86.3 GB/sec	8 x 16-bit LPDDR4x-4266 86.3 GB/sec	8 x 16-bit LPDDR4x-4266 86.3 GB.sec
Wi-Fi	Wi-FI 7 + BE 5.4 (Discrete)	Wi-Fi 6E + BT 5.1	Wi-Fi 6 + BT 5.1	Wi-Fi 5 + BT 5.0
Modem	Snapdragon X65 (Discrete)	Snapdragon X55/X62/X65 (Discrete)	Snapdragon X55/X24 (Discrete)	Snapdragon X24 (Discrete)
Process	4nm	Samsung 5LPE	TSMC N7	TSMC N7

Starting with a high-level look at the chip, the Snapdragon X Elite is a high-performance SoC designed to power Windows-on-Arm laptops. Qualcomm isn't listing any official TDPs, but the company has told us that the Elite is designed to scale across a "broad range" of thermal designs. Active cooling will be needed to get the most out of the Elite, but according to Qualcomm, passive/fanless designs are possible as well, and we should expect to see some retail devices designed as such.

Qualcomm is fabbing the chip on an unspecified 4nm process. Given their previous performance issues with Samsung's 4nm line, it's a very safe bet that they're building this chip at TSMC – possibly using the N4P line. The silicon itself is a traditional monolithic die, so there is no use of chiplets or other advanced packaging here (though the wireless radios are discrete).

CPU: Oryon By The Dozen

The star of the show (if you'll forgive the pun) is Oryon, Qualcomm's new custom-designed Arm CPU core. Designed by the Nuvia team that Qualcomm acquired in 2021, Oryon is the first high-performance, fully-custom Arm CPU core created by Qualcomm in several years. And following multiple generations of lackluster Snapdragon Compute SoCs built out of Arm Cortex-A/X designs and functionally bigger versions of Qualcomm's mobile SoCs, Oryon marks a major change in direction for Qualcomm.

Being that this is a preview, there are no significant architectural details to share on Oryon at this time. We don't know the width, or various buffer sizes, execution ports, etc. But what we do know is that Qualcomm didn't aim low with this SoC – the Nuvia team was working on a server-grade CPU core prior to their acquisition, and that kind of aggressive design has carried over into Oryon as well. Which, after all, was one of the major goals of Qualcomm's acquisition, as they have desired a high performance CPU core to push them ahead of the other laptop (and eventually mobile) chip makers.
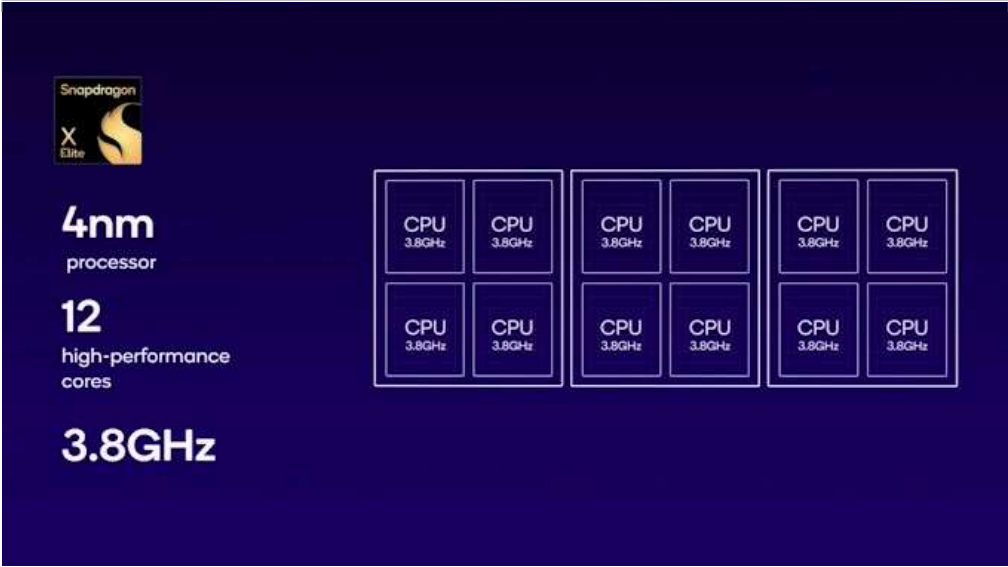
The Snapdragon X Elite SoC ships with 12 Oryon CPU cores – and that's it. Unlike Qualcomm's 8cx family of designs, there are no distinct "efficiency" and "performance" cores based on different microarchitectures; this is a homogenous CPU design, more akin to traditional PC processors. This means that Oryon needs to pull double duty, excelling in performance in heavy workloads without chewing up a bunch of power in light workloads.

The Oryon CPU cores are broken up into three clusters of 4 cores each. We're still waiting on further technical details, of course, but it's a safe assumption that each cluster is on its own power rail, so that unneeded clusters can be powered down when only a handful of cores are called for.

Just on this basis alone, Snapdragon X Elite looks like a far more potent performer than the 8CX chips it replaces. The 8cx Gen 3 offered just 4 performance cores (Cortex-X1) and another 4 eficiency cores (Cortex-A78), so Snapdragon X Elite will hit the streets with 50% more CPU cores never mind the higher performance of those cores. For a laptop chip, Qualcomm is throwing a lot of CPU cores at the matter.

With regards to clockspeeds, in an all-core turbo workload, all 12 Oryon CPU cores can hit run at up to 3.8GHz, power and thermal headroom permitting. Meanwhile in lighter workloads, the chip supports turboing up to 4.3GHz on 2 cores. Qualcomm's slide on this matter shows a core from each cluster, but it's unclear whether this is some kind of prime/favored core in action (where only certain cores are designed/validated for those speeds) or if it's simply a stylistic choice.

Either way, Qualcomm is aiming to turbo to relatively high clockspeeds for their laptop chip, a notable distinction from their much more modestly clocked 8CX chips. While high clockspeeds alone do not make for

Memory: 128-bit LPDDR5x

Feeding the beastly Oryon CPU cores (as well as the rest of the chip) is a 128-bit LPDDR5x memory bus. This is less remarkable than the CPU side of the chip, but it's important to note all the same. With the previous 8CX chips only supporting LPDDR4x, this brings Qualcomm back to parity with the latest PC chips in terms of memory technology support. And with supported data rates as high as LPDDR5x-8533, this will give Qualcomm one of the fastest memory controllers on the market.
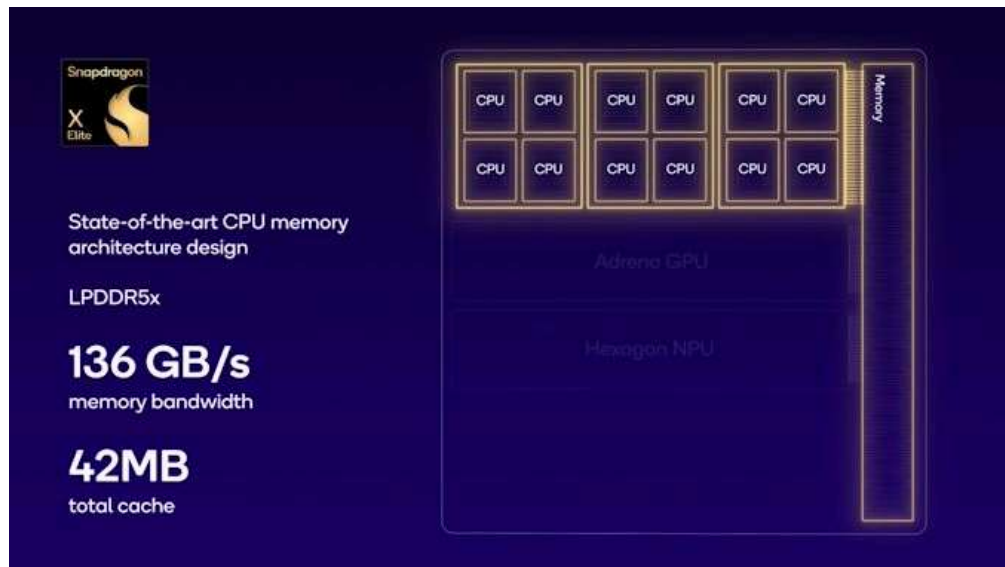
Qualcomm is also quoting a total of 42MB of cache in the system sitting between the various processor blocks and system memory. Given the explicit mention of "total cache", this is almost certainly L2 + L3. Previous Qualcomm designs have offered a 6MB shared L3 (last level) cache. If that's the case again here, then that would mean there's 3MB of L2 cache available for each CPU core – or some permutation thereof.

GPU: Latest Generation Adreno

On the graphics side of matters, Snapdragon X Elite incorporates Qualcomm's latest generation Adreno GPU. As is typical for Qualcomm in these matters, the company is saying virtually nothing about the architecture employed here, though it goes without saying that this is the latest and greatest iteration of Qualcomm's in-house GPU design.

From a feature perspective, this is a DirectX 12-class GPU with ray tracing support, mirroring the capabilities Qualcomm introduced with last year's Snapdragon 8 Gen 2 mobile SoC. Within the Windows ecosystem, it will almost certainly qualify as a DirectX 12 Ultimate (feature level 12_2) design.
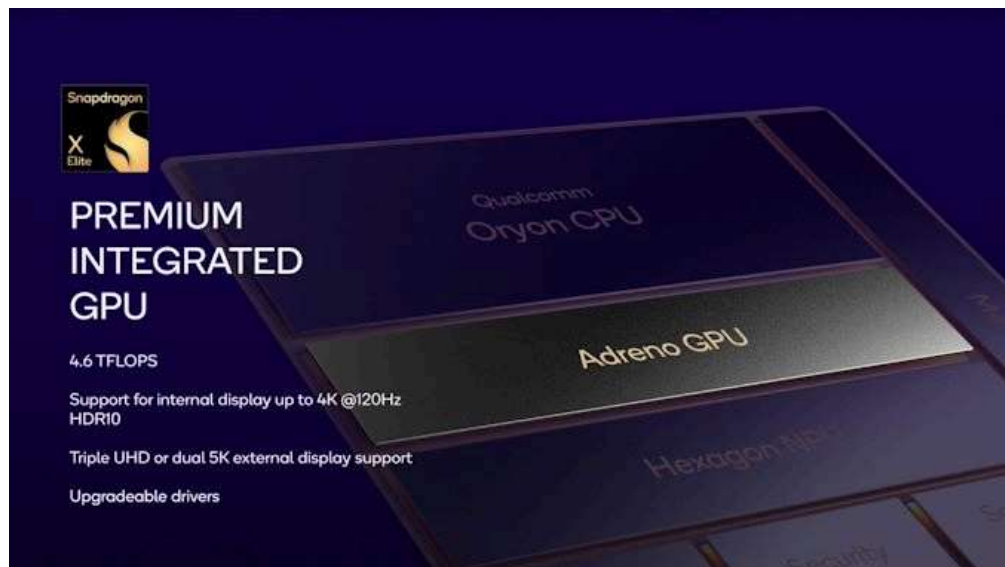
say how this will compare. Or even how it will compare to other integrated GPUs, since there's a lot more to real-world GPU performance than pure FLOPS.

The display controller portion of the GPU offers support for up to 4 DisplayPort displays. Besides an internal display for the laptop, it can drive a further 3 external displays (all DP 1.4), with one output being 5K capable, while the rest are 4K.

Finally, the SoC is getting Qualcomm's latest video processing block (VPU) as well. This latest design not only support AV1 decoding, but in a first for a Qualcomm SoC, AV1 encoding as well.

NPU: Hitting Hard with Hexagon

Next to the use of Oryon CPU cores, Qualcomm's other big bet with the Snapdragon X Elite SoC is on the AI/neural processing unit side of things with their latest generation Hexagon NPU. Qualcomm is expecting that AI use will continue to rapidly grow over the next few years, and that the next big push is going to be AI models running locally on users' systems. So they have invested a significant amount of resources in bulking up their Hexagon NPU for this generation of chips (X Elite and 8 Gen 3).

The end result is a heavily revised NPU, which should greatly exceed the 8CX Gen 3's NPU performance. Qualcomm is quoting 45 TOPS of performance here for modest precision INT8, whereas 8CX Gen 3 was previously quoted at 15 TOPS for an unspecified data format.
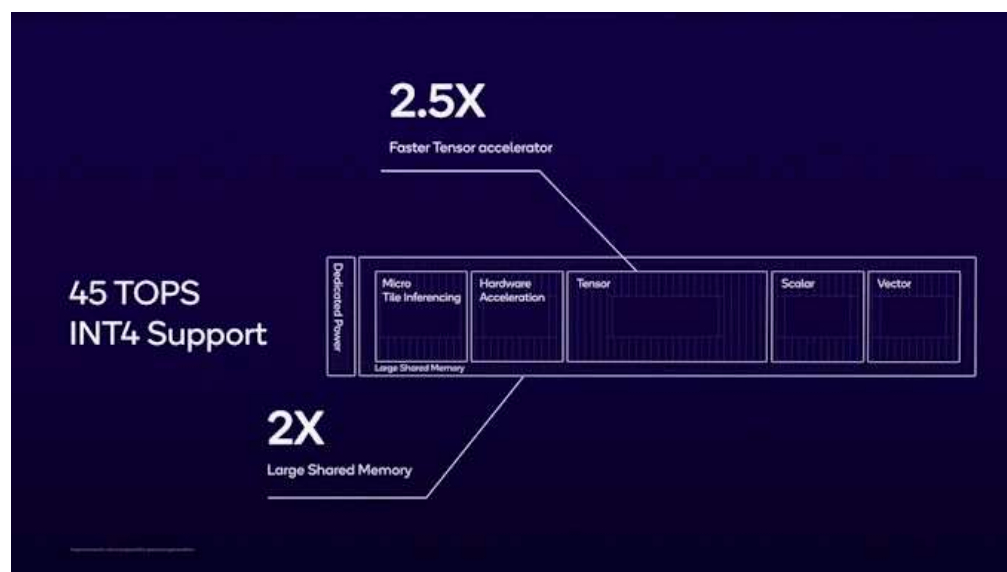
Unlike their CPU and GPU, Qualcomm is sharing some architectural details here about the NPU, and what they've done to boost its performance. The tensor accelerator block, used in the densest matrix math, is outright 2.5x faster than before. Backing that (and the rest of the NPU) is a 2x larger shared memory/cache (though Qualcomm is not disclosing the actual size). Qualcomm is targeting large language models (LLMs) in particular with this change, as these are notoriously memory bound; according to the company, the chip will have enough resources to run a 13 billion parameter Llama 2 model locally.

Qualcomm has also made some power delivery changes to help drive more performance/efficiency out of the NPU. The power-hungry tensor block is now on its own power rail, with the rest of the NPU sitting on a separate shared rail. The company has also made some further undisclosed improvements to how they handle micro-tiling of inferencing workloads, which directly impacts how well they can split up workloads to keep the various sub-blocks of the NPU as busy as possible while minimizing intermediate memory operations.

I/O: USB4, PCIe 4, & Discrete Wi-Fi 7

Rounding out the Snapdragon X Elite, let's talk I/O.

For internal I/O, the SoC offers PCIe 4.0 connectivity for NVMe storage. Elsewhere, the company is using PCIe 3 to supply connectivity to their modem and Wi-Fi solutions. No mention has been made of whether there are any free PCIe lanes for further peripherals.

As noted earlier, both Wi-Fi and the modem are discrete for this product. The chip is intended to be paired with Qualcomm's FastConnect 7800 silicon in the form of an M.2 card. The 7800 is their latest-generation Wi-Fi 7 solution, with support for 4 spatial streams as well as Bluetooth 5.4. The modem pairing is the Snapdragon X65, a high-performance 5G modem which was also available for the 8CX Gen 3.

The fact that neither wireless system is integrated into the SoC is unusual for Qualcomm, but perhaps not too surprising since they want to bring the Elite to market ASAP. Integrating these modules would take further time, and as a laptop SoC, Qualcomm doesn't need to be as space efficient. In any case, the official line from Qualcomm is that the discrete modem is for OEM flexibility – to give OEMs the option to either include a modem or not – though Qualcomm of course will be strongly encouraging OEMs to include one as a major feature differentiator of the platform.

Performance Claims

As we don't have enough architectural details to make any meaningful performance projections, the best thing we have for now are Qualcomm's vague comparisons to their competitors. This is also the closest thing Qualcomm has provided to energy efficiency data for the chip (though, as always, target clockspeeds for a SKU play a massive part there).

With 12 performance cores, Qualcomm is pushing hard on multi-threaded performance. In fact, multi-threaded performance is the only CPU performance comparisons Qualcomm makes, as there are no single-threaded comparisons to speak of. Make of that what you will.
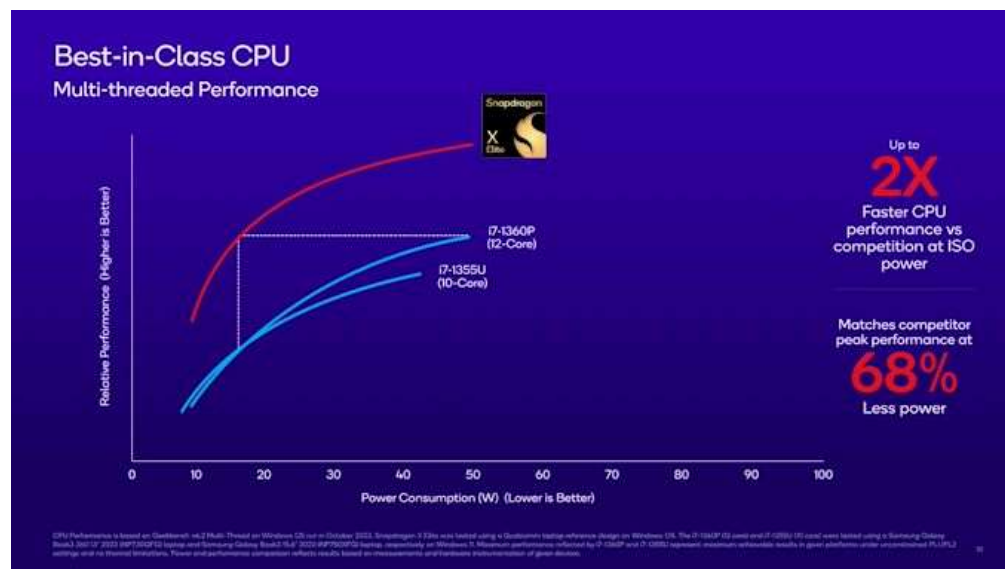
Against what is implied to be an Intel 12 core mobile CPU design, Qualcomm is reporting that Snapdragon X Elite delivers 2x the multi-threaded performance in Geekbench 6. Or at iso-performance, they hit the same mark at one-third the power consumption.

Even against Intel's best 14-core (H-class) chips, Qualcomm still reports that they lead by 60% in performance, and again are consuming one-third the power at iso-performance. Undoubtedly, a lot of this is down to the process node used, as TSMC N4 should be delivering a significant advantage over the Intel 7 process used on Intel's current chips. This is also why the "moving target" aspect is so critical, as Snapdragon X Elite should be competing with the Intel 4 based Meteor Lake lineup by the time it launches next year.

More interesting, perhaps, is that Qualcomm is reporting a 50% multi-threaded performance advantage over an unspecified "Arm-based competitor," This is meant to imply Apple, but depending on just how vague Qualcomm wishes to be, MediaTek does offer some Windows-on-Arm chips as well.
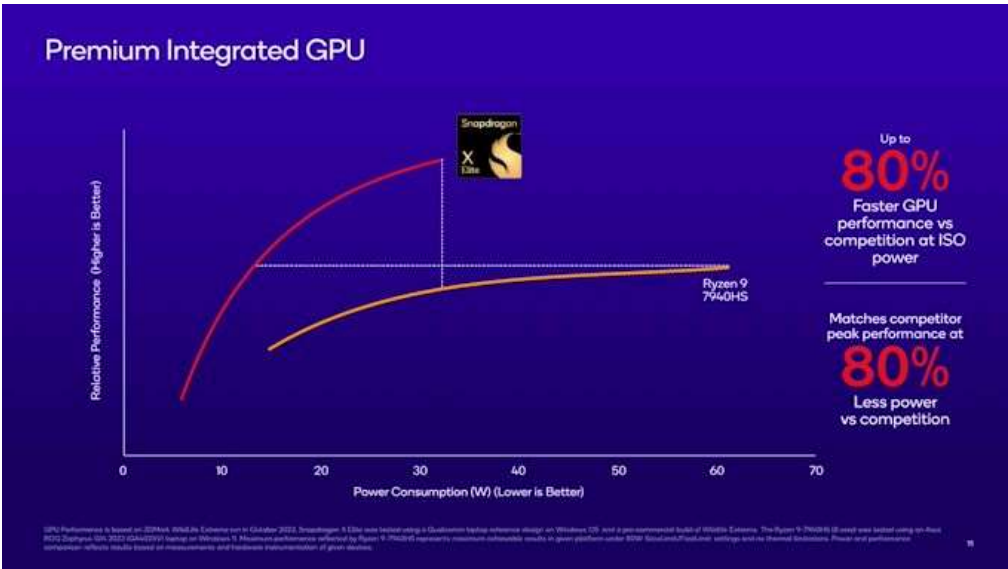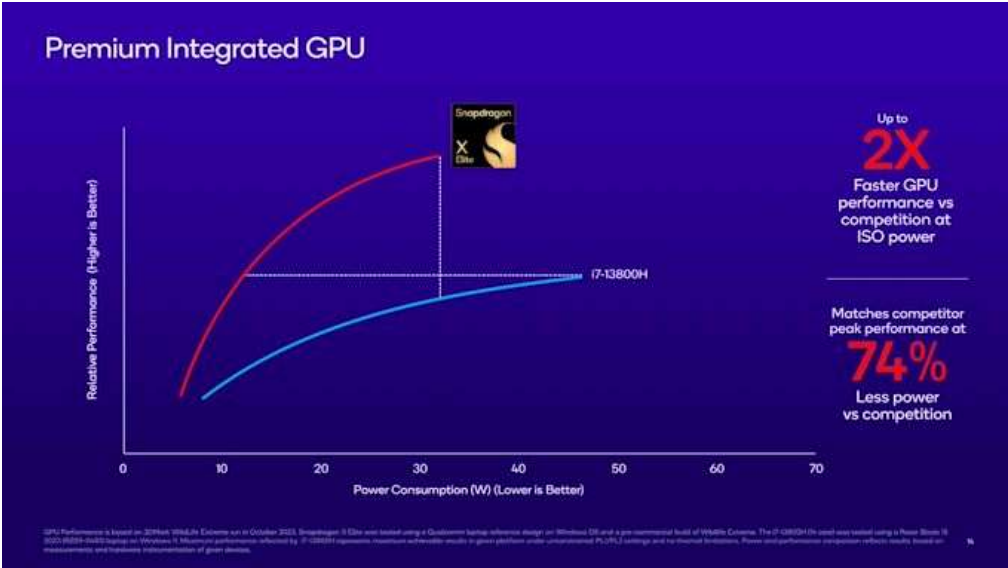
Qualcomm also expects to lead in GPU performance in 3DMark Wildlife Extreme. Which again, with a process node advantage and a tendency to build bigger iGPUs overall, is not surprising.

As always, these claims should be taken with a large grain of salt, especially for a platform that is still several months away from launching.

Snapdragon X Elite: Coming Mid-2024

Wrapping things up, Qualcomm is at this point putting the final touches on the Snapdragon X Elite. The company has deemed it one of their "most pivotal platform announcements in the company's recent history", and for good reason. The Oryon CPU core being introduced here will eventually be at the heart of a good deal more products, so how competitive Oryon is will make or break Qualcomm's next few generations of designs.
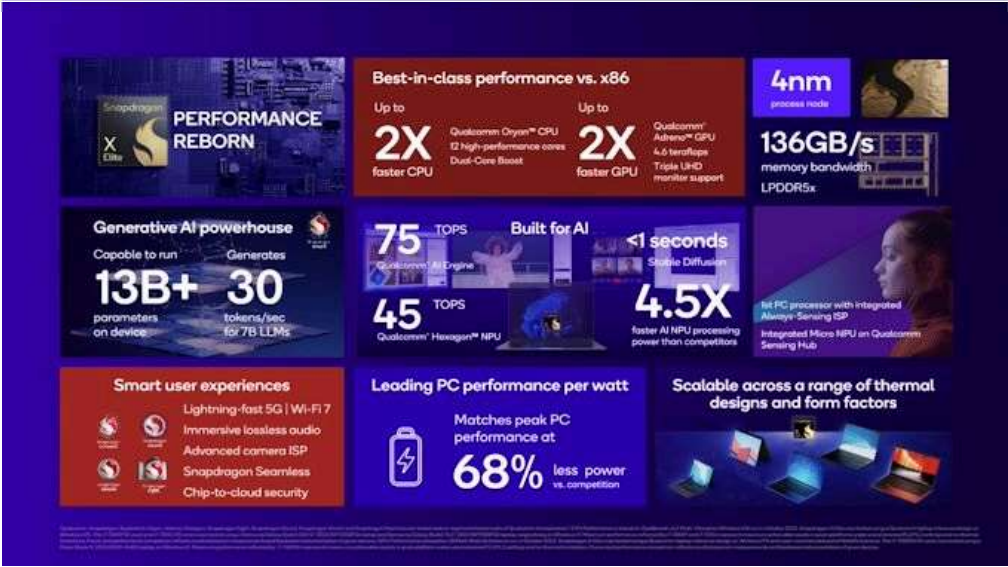
Devices based on the Snapdragon X Elite should be available in mid-2024. Which on that schedule, should see the Snapdragon X Elite competing against Intel's Meteor Lake (Core Ultra) chips, AMD's Phoenix chips (Ryzen Mobile 7000), and whatever the latest available iteration is of Apple's M-series chips.

Gallery: **Snapdragon X Elite Press Deck**
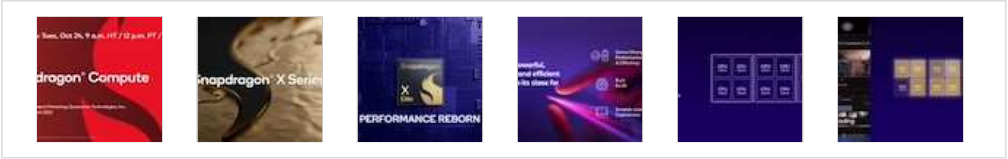
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quiksilvr - Tuesday, October 24, 2023 - link
Glad to see some competition in this space and legit laptop CPUs now and not just slightly overclocked phone chips.

garblah - Tuesday, October 24, 2023 - link
The AV1 ENCODING capability on chip is unexpected. I wonder how it will compare to hardware AV1 encoding of the latest gen of desktop GPUs.

PurposelyCryptic - Tuesday, October 24, 2023 - link
I still wouldn't want it in my laptop, I just don't trust ARM to play well with all my software.

But, assuming the GPU has no issues beating the now fairly elderly one in the Nvidia X1 SoC, give me a new Nvidia Shield TV with this kind of power, and I will start tossing money by the bagful.

I know, they specifically made this for Windows laptops, but I already have Windows laptops that more than fulfill all my laptop and laptop-related needs, in every shape and size.

But my Shield Pro and Shield tubes are starting to show their age, and this, this is the kind of power that could keep a new version future-proof for a good long while.

Would it be complete overkill, and way more expensive than what 99% of humanity would be willing to pay for an Android TV box? Of course. But I still want it. Nvidia has been dragging their heels on this, and if they don't want to make their own new SoC, just buy it. Of course, we wouldn't be getting anything as small as the tube with this anymore, but something Roku Ultra sized, at minimum. But who cares? Just

Software is also my concern but not compatibility. I have a snapdragon 8cx gen3 system and it's fine for all the software I use but once the GPU goes above 50% load the whole system crashes and I can't figure out why. No logs, no temperature sensors or voltage sensors I have been able to access. It could be a driver issue but there's only been one update since launch. It's a shame as the GPU feels competitive for an iGPU up until it crashes (e.g. half life 2 at 5120x1440 is no problem).

If it's a driver issue Qualcomm haven't released a fix. If it's something else monitoring software hasn't caught up with the platform when I last checked. I'd love a newer generation chip but it has to be better supported.

Mantion - Thursday, October 26, 2023 - link

My guess is you are using windows. Switch to an Arch based or NIX linux.

CampGareth - Thursday, October 26, 2023 - link

Good idea but for one this is the official Windows on ARM 2023 dev kit so you'd expect it to be stable and well supported under Windows. For two since it's ARM switching OS isn't anywhere near as easy as x86.

pmeinl - Thursday, October 26, 2023 - link

I too experience graphics (driver) problems with my Windows Dev Kit 2023 ARM Mini-PC. When playing YouTube videos in Firefox the driver frequently restarts, resulting in the screen going black or white. In Edge the Edge Windows flickers shortly.

In addition I sporadically I get the message (audio renderer error, please restart your computer". Windows Sandbox crashes every time when maximizing its Window (might be related to the uncommon resolution 3840×2560 of my MateView 28 monitor).

Windows Sandbox performance is barely acceptable and unpredictable. Sometimes even the volume control is extremely slow to open or does not open at all. I assume other virtualization solutions have similar problems, but did not test this.

MS did not fix all these problems in a year with three firmware updates.

domboy - Friday, October 27, 2023 - link

This is why I'm rather excited about the rumor of nVidia getting back into the Windows on ARM game. They have much more experience writing windows graphics drivers than Qualcomm. Not saying the latter is horrible, but Qualcomm doesn't even currently have proper OpenGL support in Windows.

lordlad - Thursday, October 26, 2023 - link

i reckon a new Shield TV refresh will be announce after the release of the Next Nintendo Switch followup next year and the Shield TV refresh will probably uses the binned SOC from the switch followup as its internal.

Mantion - Thursday, October 26, 2023 - link

Considering Nvidia plans on making their own desktop chips Not sure why people think a Shield refresh would have a qcom chip.

1   2   3   4   5   6   ▶

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EXHIBIT 18

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

ARM LTD., a U.K. corporation,

           Plaintiff,

      v.

QUALCOMM INC., a Delaware
corporation, QUALCOMM
TECHNOLOGIES, INC., a
Delaware corporation, and NUVIA,
INC., a Delaware corporation,

           Defendants.

C.A. No. 22-1146 (MN)

**CONTAINS HIGHLY
CONFIDENTIAL – SOURCE
CODE-ATTORNEYS' EYES
ONLY**

**REPLY EXPERT REPORT OF DR. SHUO-WEI (MIKE) CHEN
TO DR. ANNAVARAM'S REBUTTAL EXPERT REPORT**

I.   INTRODUCTION

1.   My name is Dr. Shuo-Wei (Mike) Chen and I have been retained as an expert witness on behalf of the Plaintiff Arm Ltd. in this matter.

2.   I have been asked to review the Rebuttal Expert Report of Dr. Murali Annavaram ("Annavaram Rebuttal" or " Annavaram Reb."), including materials Dr. Annavaram cited and considered. Should additional relevant documents or information be made available to me, I may adjust or supplement my opinions as appropriate.

3.   On December 20, 2023, I submitted an Opening Expert Report in this matter ("Chen Report" or "Chen Rep.").

II.   EXPERIENCE AND QUALIFICATIONS

4.   My qualifications are summarized in Section II of the Chen Report, which I incorporate by reference in this report.

III.   MATERIALS CONSIDERED

5.   In addition to my personal knowledge and expertise in the field, I have reviewed RTL source code produced by Qualcomm in this case. (*See* Chen Rep. § III.) I have also included a list of materials considered as Exhibit A to this report. These include, but are not limited to:

- The materials I considered in forming my opinions in my Opening Report, which are summarized in Section III of the Chen Report.

- Dr. Colwell's Opening and Rebuttal reports, including cited documents.

- Dr. Annavaram's Opening and Rebuttal reports, including cited documents such as QSC2ARMVQ0000120-247 and QSC2ARMVQ0000068-119.

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IV.   ANALYSIS AND OPINIONS

A.   Summary of Opinions

6.   Dr. Annavaram uses the phrase "████████ Design" to refer to Nuvia's design of the █████ core "existing at the time of the Nuvia acquisition." (Annavaram Reb. ¶ 3 & n.1.) Dr. Annavaram uses the phrase "Qualcomm Cores" to refer to "(1) one of the █████ Family of Cores (i.e., the ███████████████ ██████████████████████████████████████) and (2) the █████ Family of Cores." (Annavaram Reb. ¶ 3.) For clarity, I will use Dr. Annavaram's definitions where appropriate. I also refer collectively to the ████ █████ Design and the █████ Family of Cores as the "█████ cores."

7.   Dr. Annavaram critiques my quantitative and qualitative analysis, but does not dispute my conclusion: ██████████████████████████████████

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B.   **Quantitative Approach:** ████████████████████
████████████████████████

1.   **Summary of Dr. Annavaram's Opinions**

8.   Dr. Annavaram does not dispute the result of my quantitative

analysis: ██

███████████████████ (Annavaram Reb. at ¶¶ 253-254.) Instead, Dr.

Annavaram characterizes my analysis as "unreliable" for three reasons. First, Dr.

Annavaram opines that my analysis "ignored a majority of Qualcomm's Codebases";

second, Dr. Annavaram opines that I "omitted critical folders and files"; and third,

Dr. Annavaram opines that I used the incorrect skew tolerance. (Annavaram Reb.

at ¶¶ 258-259.) I disagree.

9.   As an initial matter, while Dr. Annavaram opines that the March 14,

2021 Nuvia █████ code is █████████████████████, Dr. Annavaram

freely admits that the same code is ████████████████████████

████████████████████████ (Annavaram Reb. at ¶ 255.)

10.   ██

██

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██

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> **2.**   **Focusing on RTL Folders for the** ████████ **Cores is**
>   **Proper**

11.   Dr. Annavaram does not dispute that RTL analysis is proper to

analyze the ████████ cores. Rather, Dr. Annavaram's primary critique is that the

way I analyzed the RTL is "unreliable." (Annavaram Reb. at ¶ 259.)

12.   Dr. Annavaram does not dispute that RTL code is the ultimate

descriptor of the underlying hardware and physical implementation of circuitry, and

that it is proper to compare RTL versions to determine the likeness of two CPU

designs or implementations. Indeed, RTL files are directly synthesized into digital

circuitry, then taken through a process to place and route the digital circuitry into a

physical silicon layout. Everything about a core's circuitry and design, and

corrections through verification to that core, are captured by the core's RTL.

Therefore, examining the RTL of a core is the most direct method of analysis, and

Dr. Annavaram does not dispute this point.

13.   Dr. Annavaram's critique is that—somehow simultaneously—my

analysis was too broad and too narrow. (Annavaram Reb. at¶¶ 260-68.) Dr.

Annavaram states that my analysis was too broad because it is not constrained to

"code that is allegedly ████████████████████████████████

(Annavaram Reb. at ¶ 260.) In other words, Dr. Annavaram requires me to identify

code that is ████████████████████ before I analyze it. Dr. Annavaram has

it backwards: my analysis is intended to *identify* code that is ████████████

████████ Dr. Annavaram's critique is illogical, as it asks me to conclude what is

████████████████████████ Further, Dr. Annavaram fails to specify those

portions of the code he might believe are not ██████████████████████.

14.   Dr. Annavaram also opines that my analysis was too narrow.

(Annavaram Reb. at¶¶ 260-68.) I disagree. I focused on the folders implementing

the ██████ cores. If the core is ████████████████████████████████

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█████

15.   In my opening report, I note that I was able to find the folders and

RTL files that correspond to the key building blocks of the ██████ cores and that I

excluded folders and files that are not direct indicators of the ██████ core's use of

architectural elements from the Arm ARM. (*See* Chen Rep. ¶¶ 26-29.) My analysis

followed this procedure because the Arm ARM is an architecture-compliance

manual for the core design, and it would be a tangential exercise to compare aspects

of an SoC design which are not directly reflective of the Arm ARM implementation,

such as C/C++ software files. (*See* Chen Rep. ¶¶ 26-29; Annavaram Reb. at ¶ 263

(suggesting software C/C++ files should be analyzed further).) Dr. Annavaram

further ignores that the addition of ██████████████████████████████

███

████████

16.   I disagree with Dr. Annavaram that "by selecting a limited set of folders and files . . . Dr. Chen's analysis is unreliable." (*See* Annavaram Reb. at ¶ 260.) My analysis is reliable precisely because I filtered out certain folders and files, such as those related to SoC components that are not ████████████████ ████████ I compared the RTL files and folders for the ██████ cores across versions because it is the ██████ cores that are governed by the Arm ARM in implementing functionality compatible with Arm ISA. My approach of selecting specific folders and files from the ██████ core RTL allows for a thorough examination of Arm compatibility in an efficient manner.

17.   Dr. Annavaram incorrectly attempts to shift the focus from the main ██████ core design files to folders and files that I exempted from analysis, and which are not relevant or have low relative relevance to Arm compatibility, such as "(1) all SoC related directories, (2) all the ██ related directories that are outside the ████████ folder, and (3) certain folders within the ████████ folder itself." (Annavaram Reb. at ¶ 261.) Dr. Annavaram further points to components excluded from my analysis such as SoC code relating to the ██████████████████████ ██. (Annavaram Reb. at ¶¶ 262-63.) Again, whether these folders and files are ████████ would not change those that are, as my analysis shows.

18.   In determining whether the original Nuvia ████ Core, i.e. the main

CPU core, was based on the Arm ARM and Arm's architecture (and later whether

Qualcomm's Cores are based on the same), it is unnecessary to include everything

needed to develop, build, and test the entire SoC, such as "the code for executing the

███████████████████████," "code for the ████████████," and ██████████

████████████. (Annavaram Reb. at ¶¶ 262-63.) These may be necessary to

develop an SoC, but the architecture used by the internal CPU can be directly

revealed without focus on these components, and (as noted) whether these

components are ████████ does not change the nature of those that are.

19.   I further disagree with Dr. Annavaram that my exclusion of the

████████ folder (comprising ████████) results in an uncomprehensive analysis.

(Annavaram Reb. at ¶¶ 264-65.) These files are tangential to determining the

extent of Qualcomm's use of the Arm Architecture in the ██████ cores. It is more

direct to analyze the relevant RTL code I identified in my opening report, which

necessarily captures any design changes implemented as a result of verification and

test efforts stemming from use of the ██████ files. Likewise, Dr. Annavaram

suggests I should have included folders and files relevant to blocks outside the CPU

core such as ████████████████████████████████████ (Annavaram

Reb. at ¶ 266.) Again, these components are tangential to the specific analysis , as

they only support the CPU core. Indeed, a functioning CPU could be Arm-compliant

and not have these components.

20.   To be clear, while Qualcomm/Nuvia's SoCs contain other components, blocks, and units outside of the ███████ cores, the SoCs ultimately ████████ ██ ██

21.   I am not aware of any circumstances in which an SoC utilizes Arm-based CPU cores while the other components of the SoC support a non-Arm architecture. In my opinion, to develop such a system would be exceedingly difficult and expensive, at the risk of the CPU and SoC not being functional. This further justifies the focus of my analysis on the blocks and units within the CPU core to efficiently produce reliable analysis. For example, the RTL of ████████████ ████████████████████████████████████. I focused on the ████████ ████ because it is the CPU core (██████████████████████████████████████) and provides sufficient information to examine whether it is designed based on Arm's ARM. It would be a tangential exercise to examine the ████████████ ███████████████████████████████████, or any of the other components that Dr. Annavaram suggests for further inclusion, in part because regardless of whether those components are ████████, the core would ██████████████████ ████████ (Annavaram Reb. at ¶¶ 266, 268.)

22.   I also disagree with Dr. Annavaram that my analysis should have included the "folders and files associated with the ████████" of ████ ████████████████████ (Annavaram Reb. at ¶ 267.) The ████████ is irrelevant to my analysis of Arm compliance and ██████████████████████████ In

-8-

my opening report, I was able to determine that the main CPUs were ████████

███

███
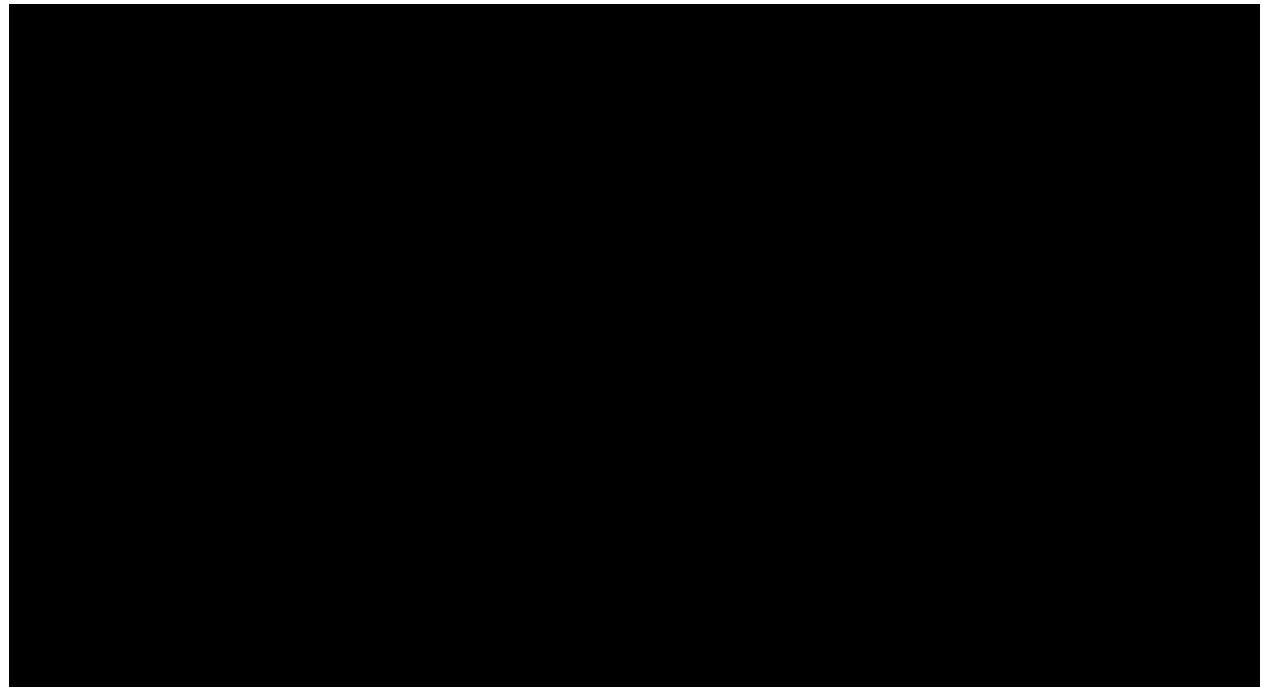
      23.   Dr. Annavaram is incorrect that my analysis should have included the

additional folders and files he notes. As explained in my opening report, I selected

the relevant folders and files by relying on Nuvia and Qualcomm's own technical

documents that identify the design hierarchy and file locations for the ████████

cores. For example, QCARM_2414840 shows an ██████ SoC containing the ██████

██

(QCARM_2414845.)

(QCARM_2414842.)

24. As explained in my opening report, I examined the ███████ of the design hierarchy that contain the █████ CPU core: ███████████████ █████████████████████████████████ (Chen Rep. at ¶¶ 28-32.) Consequently, I examined the most relevant top-level RTL files and the associated RTL files within the CPU block or unit. These design hierarchies and RTL file locations are provided in QCARM_2551809, excerpted below. Based on this information, there was no need to investigate folders and files other than those I identified in my opening report, because they sufficiently demonstrated the ████████████████████████ in part via highly similar Arm-compatibility RTL code across the ███████ designs.

-11-
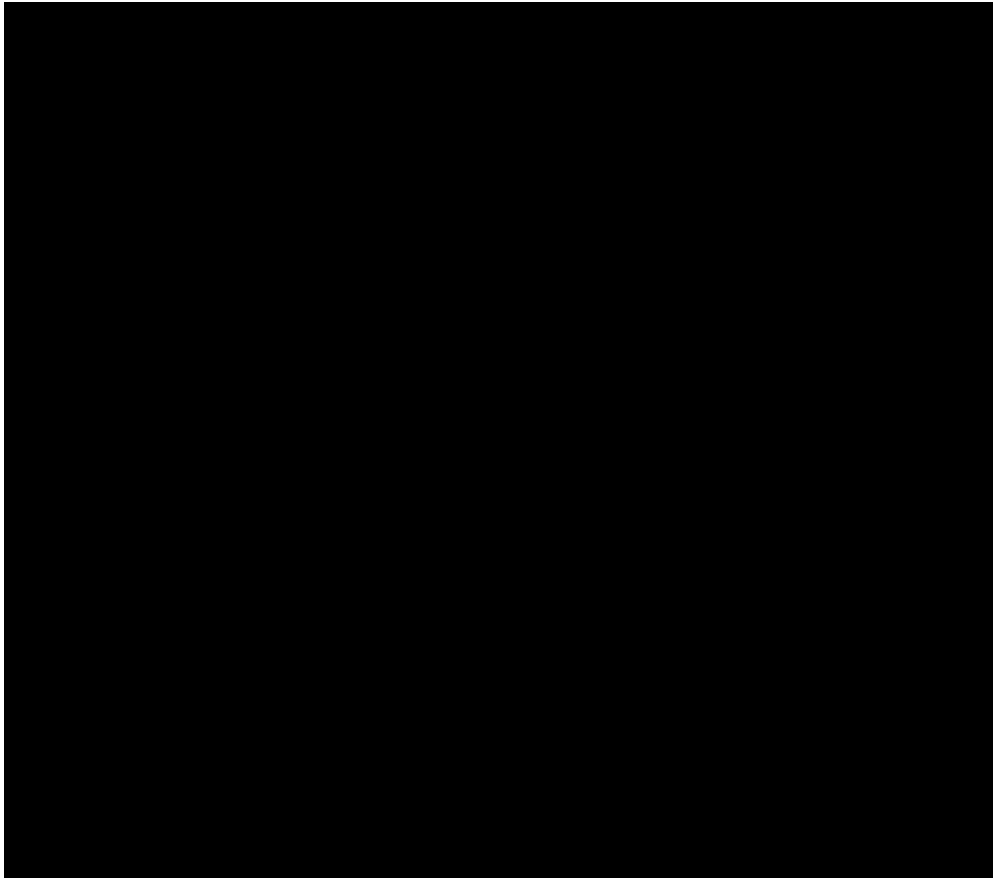
(QCARM_2551819.)

(QCARM_2551820.)

ny-2699569
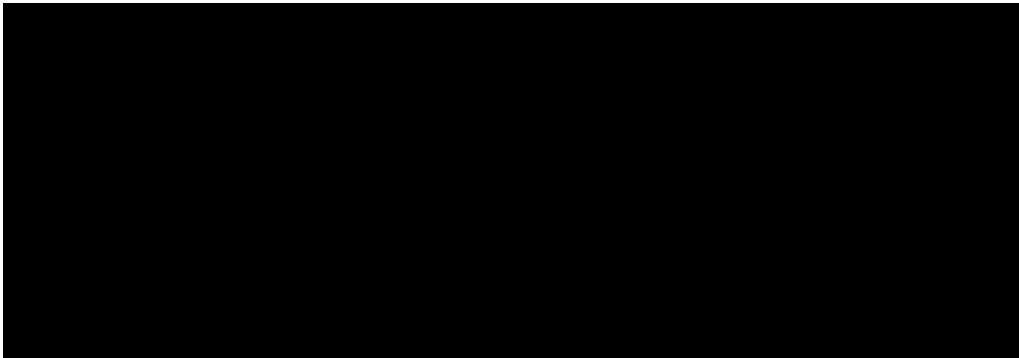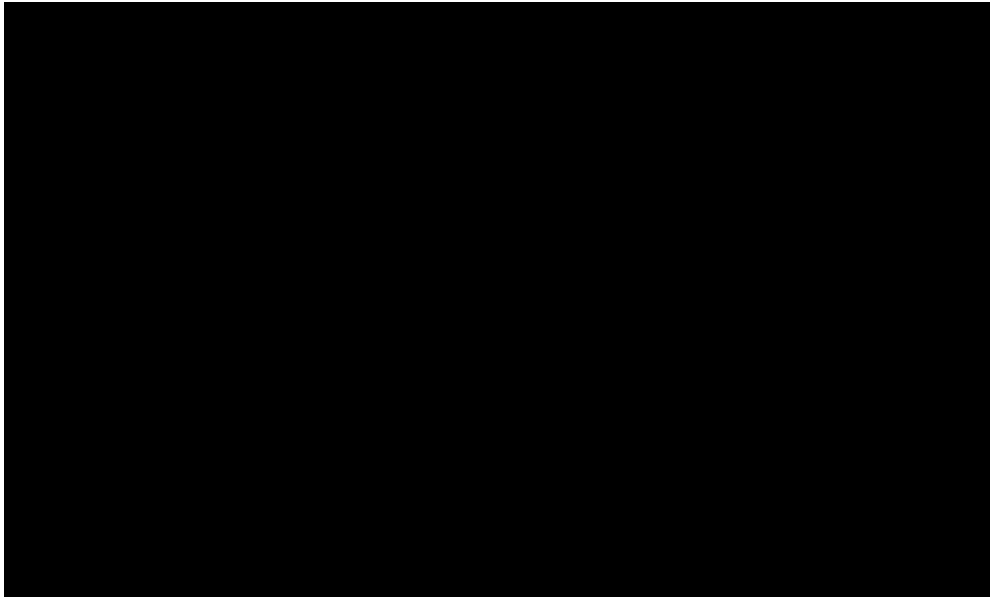
(QCARM_2551823.)

3.   The Chosen Skew Tolerance is Proper

25.   Dr. Annavaram also claims that my "qualitative comparisons are meaningless" because of the skew tolerance that was used in the Beyond Compare tool.

26.   In my opening report, I explained that I compared the ███ codebase version just prior to Qualcomm's acquisition of Nuvia (March 14, 2021 version) against all subsequent versions of the code produced by Qualcomm. (Chen Rep. at ¶¶ 24-25.) I explained further that I used a tool called Beyond Compare to perform this analysis with its default skew setting of 2,000, which means the tool would search up to 2,000 lines above or below the current line for a matching line. (Chen Rep. at ¶ 27.) Dr. Annavaram admits that 2,000 is the default skew tolerance in Beyond Compare. (Annavaram Reb. at ¶ 271.)

-12-

27.   Dr. Annavaram does not explain why he does not agree with the default skew tolerance value. Dr. Annavaram appears to prefer a lower skew tolerance value, but a lower skew tolerance is **less accurate** than a higher skew tolerance. This is because skew tolerance permits the program to compare more lines of code. Ideally, a true compare would have a skew tolerance of infinity. However, higher skew tolerances require more processing time, as the program has to compare more lines of code. Accordingly, tools such as Beyond Compare have a default skew tolerance of 2,000, which represents a middle ground between accuracy and efficiency. This is confirmed by the developer of Beyond Compare[1]:

> Choose a Skew tolerance value to specify the maximum number of lines that the algorithm will check when looking for a match to a particular line. Increasing the setting can improve the alignment, especially if there are large gaps. Of course, the comparison may also require more time.

28.   I disagree with Dr. Annavaram that the default skew tolerance of 2,000 "is simply an inaccurate parameter" and that it should have been set lower, to a value of 100 or even 0. (Annavaram Reb. at ¶¶ 269-279.) As an initial matter, each line of RTL code is typically quite particularized and would be unlikely to appear in two separate files unless the RTL code is indeed exactly identical to code in a prior file.

29.   For example, a designer may first write RTL code to implement a digital adder at a particular line location (line N). If the designer later changes the line location of that RTL code (to line N+1), e.g. by inserting a single comment above

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[1] Beyond Compare, https://www.scootersoftware.com/v4help/sessiontextalignment.html, (last visited March 24, 2024).

ny-2699569

the RTL code, the Beyond Compare tool would not identify a match for any code below that comment when set with a skew of 0. In this example, two identical files (offset by one line) could yield a near 0% match by changing only one line of code in any size file. Dr. Annavaram's suggestion to use a skew of 0 is therefore meritless, and his suggestion to use a low skew of 100 would only introduce error.

30.   In fact, when comparing two RTL files, considering the typically particularized nature of each line of RTL code, it is best to increase the skew tolerance to be the maximum number of lines between the two files being compared, such that the Beyond Compare tool can better align and identify any identical RTL code between the two files regardless of the line location. This is an effective method for comparing the extent of which two files are identical precisely because RTL code is unique and unlikely to be reproduced exactly in a compared file unless the RTL code was copied. Therefore, Dr. Annavaram's suggestion to use a skew of 0 or 100 is unreliable.

31.   To illustrate this, I have generated two RTL files using the Verilog examples from https://www.asic-world.com/examples/verilog/index.html. In RTL_code_A.v, I implemented a multiplexer ("MUX") module and a counter module. In RTL_code_B, I only implemented a counter module, which is identical to the one in RTL_code_A.v. Therefore, RTL_code_A.v and RTL_code_B.v are identical except that RTL_code_A.v also contains a MUX module in the lines right above the counter module. I compared these two RTL files using Beyond Compare with two different settings: with the default skew tolerance of 2,000, and the other with a skew

-14-

tolerance of 2. The comparison result is shown below. The red regions illustrate

the lines with differences, according to the tool.

- Setting I: Skew tolerance of 2:

3/16/2024 11:52:47 PM   Text Compare   Page 1
Mode: All
Left file: C:\Users\Mike Chen\Documents\RTL_code_A.v
Right file: C:\Users\Mike Chen\Documents\RTL_code_B.v

```
 1 //------------------------------------    =      1 //------------------------------------
   » ----------------                              » ----------------
 2 // Design Name : mux_using_assign        <>     2 // Design Name : up_counter
 3 // File Name   : mux_using_assign.v              3 // File Name   : up_counter.v
 4 // Function     : 2:1 Mux using Assign           4 // Function    : Up counter
 5 // Coder        : Deepak Kumar Tala               5 // Coder        : Deepak
 6 //------------------------------------    =      6 //------------------------------------
   » ----------------                              » ----------------
 7 module  mux_using_assign(               <>     7 module up_counter    (
 8 din_0       , // Mux first input                8 out     , // Output of the counter
 9 din_1      , // Mux Second input                9 enable  ,  // enable for counter
                                                  10 clk      ,  // clock Input
10 sel         , // Select input                  11 reset      // reset Input
11 mux_out      // Mux output
12 );                                      =     12 );
13 //----------Input Ports---------------   <>    13 //----------Output Ports--------------
14 input din_0, din_1, sel ;                      14     output [7:0] out;
15 //-----------Output Ports-------------          15 //------------Input Ports--------------
   » -
16 output mux_out;                                 16     input enable, clk, reset;
17 //------------Internal Variables-------  =     17 //------------Internal Variables-------
   » -                                             » -
18 wire  mux_out;                          <>    18     reg [7:0] out;
19 //-------------Code Start-------------          19 //-------------Code Starts Here-------
   » ---
20 assign mux_out = (sel) ? din_1 : din_0;        20 always @(posedge clk)
21                                                21 if (reset) begin
22 endmodule //End Of Module mux                  22   out <= 8'b0 ;
23                                                23 end else if (enable) begin
24                                                24   out <= out + 1;
25 //------------------------------------          25 end
   » ----------------
26 // Design Name : up_counter                     26
27 // File Name   : up_counter.v                   27
28 // Function    : Up counter                     28 endmodule
29 // Coder        : Deepak
30 //------------------------------------
   » ----------------
31 module up_counter    (
32 out     , // Output of the counter
33 enable  ,  // enable for counter
34 clk      ,  // clock Input
35 reset      // reset Input
36 );
37 //----------Output Ports--------------
38     output [7:0] out;
39 //------------Input Ports--------------
40     input enable, clk, reset;
41 //------------Internal Variables-------
   » -
42    reg [7:0] out;
43 //-------------Code Starts Here-------
```

Beyond Compare v4 4.7

```
3/16/2024 11:52:47 PM                              Text Compare                              Page 2
Left file: C:\Users\Mike Chen\Documents\RTL_code_A.v
Right file: C:\Users\Mike Chen\Documents\RTL_code_B.v
(continued)
44  always @(posedge clk)
45  if (reset) begin
46    out <= 8'b0 ;
47  end else if (enable) begin
48    out <= out + 1;
49  end
50
51
52  endmodule
                                                                          Beyond Compare v4.4.7
```

- Setting II: Skew tolerance of 2,000 (default):

3/16/2024 11:53:35 PM   Text Compare   Page 1
Mode: All
Left file: C:\Users\Mike Chen\Documents\RTL_code_A.v
Right file: C:\Users\Mike Chen\Documents\RTL_code_B.v

```
 1 //-------------------------------------    =    1 //-------------------------------------
   » ----------------                              » ----------------
 2 // Design Name : mux_using_assign           +-
 3 // File Name   : mux_using_assign.v
 4 // Function    : 2:1 Mux using Assign
 5 // Coder       : Deepak Kumar Tala
 6 //-------------------------------------
   » ----------------
 7 module  mux_using_assign(
 8 din_0     , // Mux first input
 9 din_1     , // Mux Second input
10 sel       , // Select input
11 mux_out     // Mux output
12 );
13 //-----------Input Ports---------------
14 input din_0, din_1, sel ;
15 //-----------Output Ports--------------
   » -
16 output mux_out;
17 //------------Internal Variables-------
   » -
18 wire  mux_out;
19 //-------------Code Start--------------
   » ---
20 assign mux_out = (sel) ? din_1 : din_0;
21
22 endmodule //End Of Module mux
23
24
25 //-------------------------------------
   » ----------------
26 // Design Name : up_counter              =    2 // Design Name : up_counter
27 // File Name   : up_counter.v                 3 // File Name   : up_counter.v
28 // Function    : Up counter                    4 // Function    : Up counter
29 // Coder       : Deepak                        5 // Coder       : Deepak
30 //-------------------------------------        6 //-------------------------------------
   » ----------------                              » ----------------
31 module up_counter    (                         7 module up_counter    (
32 out     ,  // Output of the counter           8 out     ,  // Output of the counter
33 enable  ,  // enable for counter              9 enable  ,  // enable for counter
34 clk     ,  // clock Input                    10 clk     ,  // clock Input
35 reset      // reset Input                    11 reset      // reset Input
36 );                                           12 );
37 //----------Output Ports--------------       13 //----------Output Ports--------------
38    output [7:0] out;                         14    output [7:0] out;
39 //------------Input Ports-------------       15 //------------Input Ports-------------
40     input enable, clk, reset;               16     input enable, clk, reset;
41 //------------Internal Variables-------      17 //------------Internal Variables-------
   » -                                              » -
42    reg [7:0] out;                            18    reg [7:0] out;
43 //-------------Code Starts Here-------       19 //-------------Code Starts Here-------
44 always @(posedge clk)                        20 always @(posedge clk)
```

Beyond Compare v4.4.7

```
3/16/2024 11:53:35 PM                              Text Compare                              Page 2
Left file: C:\Users\Mike Chen\Documents\RTL_code_A.v
Right file: C:\Users\Mike Chen\Documents\RTL_code_B.v
(continued)
   45 if (reset) begin                     21 if (reset) begin
   46    out <= 8'b0 ;                      22    out <= 8'b0 ;
   47 end else if (enable) begin            23 end else if (enable) begin
   48    out <= out + 1;                    24    out <= out + 1;
   49 end                                   25 end
   50                                       26
   51                                       27
   52 endmodule                             28 endmodule
```
Beyond Compare v4 4.7

32.   In Setting I, with a skew of 2, Beyond Compare finds zero identical

lines of code. In Setting II, Beyond Compare correctly identifies 100% of the

identical lines of code. Had I used more complicated examples, with much larger

file sizes (over 2,000 lines), even Setting II may have failed to identify the identical

lines of code without a further increase to the skew tolerance to match the file size.

33.   From this simple exercise, it is evident that Beyond Compare would

fail to identify the same RTL code within two files as smaller skew tolerances are

used, especially with larger files. One could increase the skew tolerance beyond the

default value at the cost of a longer run time by the tool. Had I used a higher skew

tolerance than 2,000, it would likely have resulted in an even more accurate

measurement of RTL code similarity, that is, even higher similarity percentages

than what was reported in my opening report.

34.   The comparison tables generated by Dr. Annavaram that use lower

skew tolerance values, such as 100 or 0, are underreporting true similarities,

especially for files larger than 100 lines. (Annavaram Reb. at ¶ 276.) As noted, a

comparison with such a small skew will not catch identical RTL code between two

files if the RTL code was simply moved down a few pages to a new location. Such

movement is typical in RTL code when comments are added, more modules are

pasted in, modules are edited, or modules are deleted. Further, a skew tolerance

greater than the number of lines in a file does no harm, as Beyond Compare will not

search outside the compared files for identical RTL code. Therefore, Dr.

Annavaram's suggestion to use a skew lower than the number of lines in the file is

meritless. Likewise, it means little to know the mean and median number of lines

of code per file when the proper method of comparison is to use as large of a skew as

possible, and when too large of a skew has no negative impact on the accuracy of the

comparison. (Annavaram Reb. at ¶¶ 277-278.)

35.   As to Dr. Annavaram's comparison of codebases, I generally disagree

with his approach of only comparing the March 2021 ████ version against 2023

SoC codebases. Dr. Annavaram ignores earlier SoC versions, including July 2021

████ April 2023 ████ January 2022 ████ February 2023 ████████

February 2022 ████ and April 2022 ████ which are Qualcomm Cores.

(Annavaram Reb. at ¶¶ 272-274.) Dr. Annavaram did not compare the RTL code

similarity between the February 2022 version of ████ and the April 2022 version of

████ which have a high degree of similarity between the RTL codebases and

demonstrate that the ██

████████████████████████

4.   Dr. Annavaram's Own Analysis Shows ████████

36.   While I find it unnecessary to compare more blocks or units beyond the main CPU core as I explained above, Dr. Annavaram's line similarity analysis on blocks and units outside of the CPU core further supports my position. (Annavaram Reb. at ¶ 274.) The design hierarchy of the CPU core is defined by Nuvia and Qualcomm's own technical documents (e.g. QCARM_2414840). Based on this hierarchy, it makes more sense to focus on the blocks and units that were present in Nuvia's design to determine if they were inherited by Qualcomm's design, including blocks and units such as ████████████████████████ (*See* Annavaram Reb. ¶ at ¶ 274.)

37.   But even according to Dr. Annavaram's analysis, there is still ████████████████████████████████████ ████████ (Annavaram Reb. at ¶ 274.) I note that Dr. Annavaram does not specify which files and folders he included in his analysis, but the results support my conclusions. ████████████████████████ ████████████████████████████████████ ████████████████████████████████ ████████████████████████████ ████████████ ██ ████████████████ ████████████████████████████

38.   Dr. Annavaram's own analysis of the ███████ [2] file shows

███

███████████████ (Annavaram Reb. at ¶ 279; QSC2ARMVQ0000090-109.)

Dr. Annavaram never explained why he chose the ██████ file. It is likely

because it demonstrates a ████████████████████. But, for example, had

he chosen ████████, the line similarity percentage would be ████.

(QSC1ARMVQC0000101.)

39.   ██

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███████████████████████████████████

40.   Further, in preparing of my Opening Report, I did my own similarity

analysis of the ████ and ████████████ file.

(QSC1ARMVQC0000101). Using Beyond Compare and the default skew tolerance

of 2,000, I found that ████████████████████████████

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-23-

41.   Finally, Dr. Annavaram's rebuttal does not address the file name and directory structure similarity analysis I performed in my opening report other than to claim that two file names and directories could be the same but have different contents. (Annavaram Reb. at ¶ 270.) █████████████████████████

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█████████████   Dr. Annavaram does not dispute this.

(QCARM_2551823.)

ny-2699569
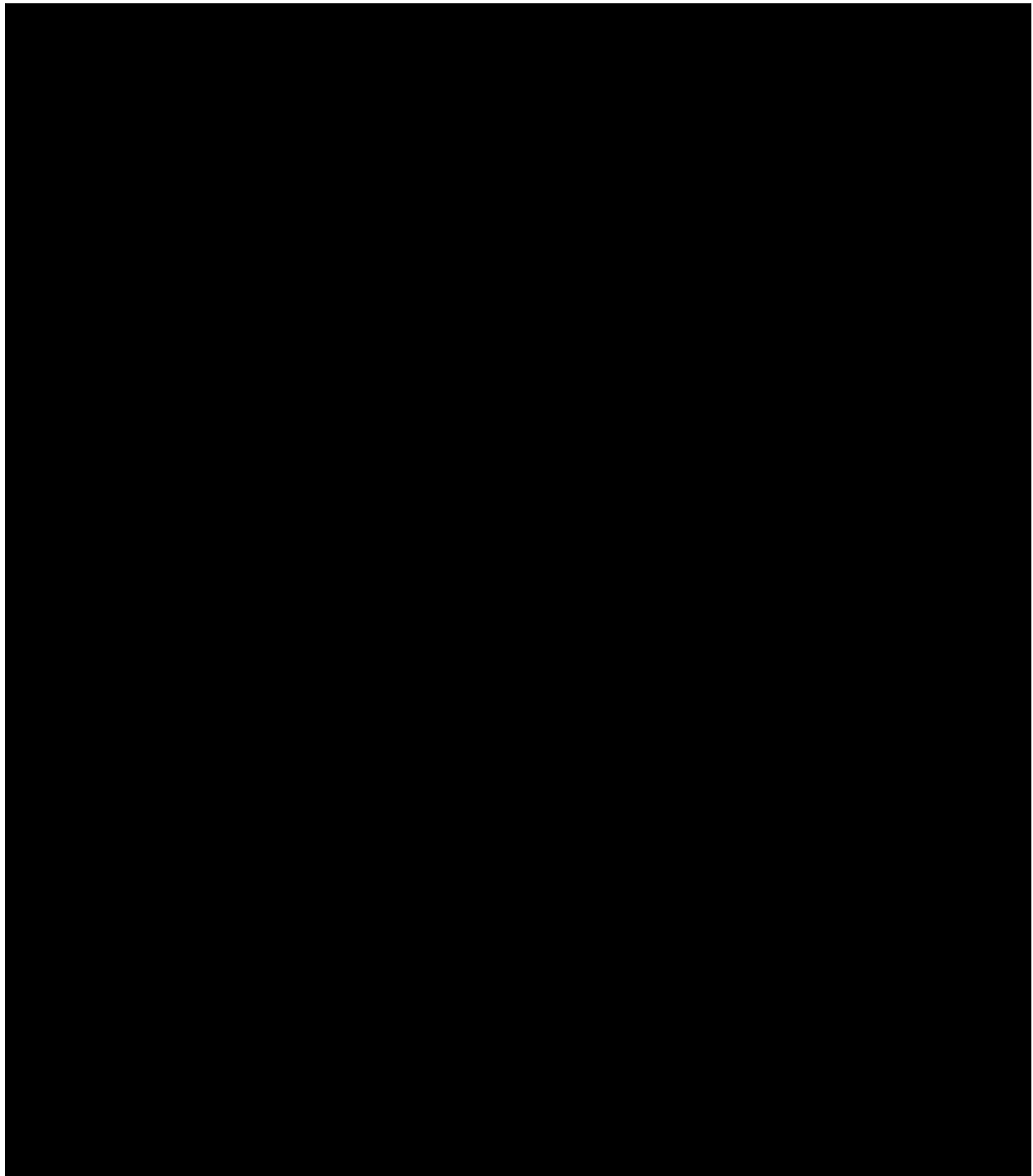
C.   **Qualitative Approach:** ████████████████
████████████████

1.   **Dr. Annavaram Agrees that** ██████████
███████████████████████████████
██████████████

42.   As explained in my opening report, I have identified the Arm features within RTL code of the Qualcomm Cores, ███████████████████████ ████████████████ (Chen Rep. at ¶¶ 36-53.) The specific way that the designers apply those ARM features to optimize the CPU performance for a particular SoC does not change the fact that it is ARM compatible and ██████████ ████████ Dr. Annavaram does not dispute this, describing these features as "compatible with Arm ARM." (Annavaram Reb. at ¶ 282.) I disagree with Dr. Annavaram that these are "independently designed." (Annavaram Reb. at ¶ 282.) To be compatible with the Arm ISA means, necessarily, that features, algorithms, and methodologies are **dependent** or based on the Arm ISA and Arm ARM.

43.   More specifically, Dr. Annavaram opines that the "█████████ was independently designed by Nuvia and Qualcomm."[3] (Annavaram at ¶ 284.) I disagree this is relevant if Dr. Annavaram cannot refute there are other ████████ aspects of the relevant cores. Further, as mentioned above, the ██████ is Arm-compatible, and thus not independently designed, free of any compliance with relevant Arm requirements. █████████████████████████████

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[3] I am not a lawyer, and thus have no opinion whether something was designed under a specific ALA.

███

██ (Chen Rep. at ¶ 39.) It is worth mentioning that even if there is only one

whitespace difference in the corresponding line between the two files, the Beyond

Compare tool will flag it as an unimportant difference line by default. In my

experience, it is extremely unlikely that two designers creating a file (███████

███████) independently would end up with ███████████████

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█████████████████████████████

44.   To illustrate this point, I used the same exemplary RTL code

mentioned in Section IV.B.3 above (*see* ¶ 31) and compared it using Beyond

Compare. Setting I (the same RTL code as Setting I in ¶ 31):

In Setting I, the Beyond Compare tool reports 28 same lines, as shown below:

Text Compare Info

28 same line(s)
3 unimportant left orphan line(s)
21 important left orphan line(s)

1 difference section(s)

Close

Setting II (the same RTL code as Setting I, except I added one extra whitespace to

line 18 of RTL_cdoe_B.v):

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In Setting II, the Beyond Compare tool reports 27 same lines, as shown below. In other words, the tool does not count the line with only one extra whitespace as the "same line."
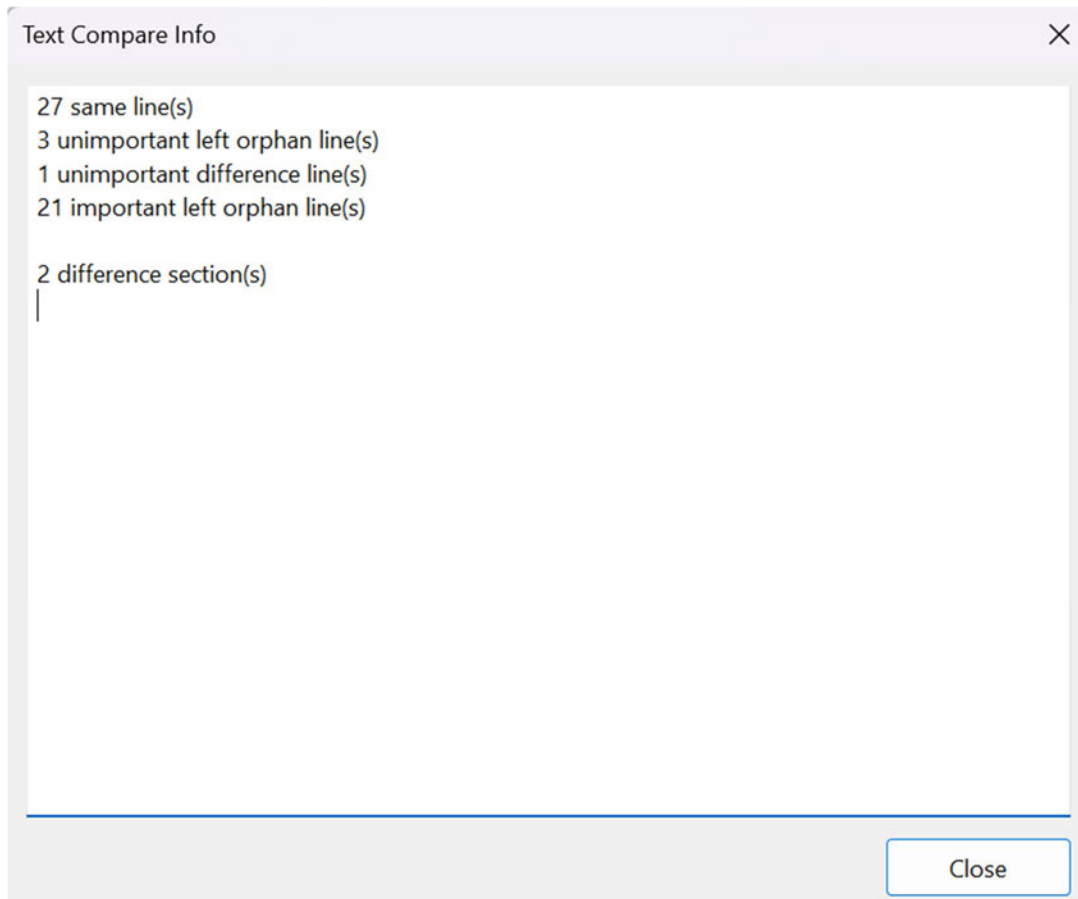
ny-2699569

```
Text Compare Info                                          ✕

  27 same line(s)
  3 unimportant left orphan line(s)
  1 unimportant difference line(s)
  21 important left orphan line(s)

  2 difference section(s)
  |

                                                      [ Close ]
```

45.   ███

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46.   ███

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47.   As I explained earlier, compatibility with the Arm ISA shows that a

design is ████████████████████████████████████ Dr. Annavaram does

not explain the basis for his statement that interoperability and compatibility does

not imply that Qualcomm's Product Designs are ████████████████████████████

██████████████████████████ (Annavaram Reb. at ¶ 285.) In my opinion,

that is precisely what interoperability and compatibility with Arm's architecture

shows: that a design is ██████████████████████████████████

48.   Further, Dr. Annavaram admits that the "Arm ARM describes how to

interpret the defined values to determine the functionalities" in the register fields.

(Annavaram Reb. at ¶¶ 286-287.) Likewise, Dr. Annavaram admits that "the

purpose of these identification registers is to enable software to understand the

level of support in hardware." (Annavaram Reb. at ¶ 288.) █████████████

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49.   As Dr. Annavaram admits, the Arm ARM "describes what functionality

the software can rely on the hardware to provide." (Annavaram Reb. at ¶ 288.)

Thus, without the Arm ARM, a designer will not know all of the functionalities

software can rely on. Dr. Annavaram's example of register ID_AA64ISAR1_EL1,

which Dr. Annavaram admits "describes the presence or absence of various

capabilities," further supports this conclusion. (Annavaram Reb. at ¶¶ 288-92.) Dr.

Annavaram's other examples similarly show the contours of what a designer is able

to implement, which is all described by the Arm ARM. That the microarchitect has

some choice in implementation (Annavaram Reb. at ¶¶ 292-94) does not change the

fact that the designer must still consult with the Arm ARM to design a functioning

processor, and that processor will be ███████████████████

     50.   Regarding compliance with ARM's architecture extensions, Dr.

Annavaram admits that ███████████████████████████████

███████████████ (Annavaram Reb. at ¶ 295.) Dr. Annavaram also admits that

this "relates to the interoperability of Qualcomm Product Designs with the Arm

Architecture." (Annavaram Reb. at ¶ 295.) As explained above, this

interoperability shows that the Qualcomm Product Designs are ███████████

███████████████████ While Dr. Annavaram asserts otherwise

(Annavaram Reb. at ¶ 295), he does not explain why.

     51.   ███████████████████████████████████████

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52. ██

53. ██

2.   Dr. Annavaram's Critiques are Meritless

54.   As described in my opening report and the previous section, my and

part of Dr. Annavaram's analysis have shown that the ███████ Design is

compatible with the Arm ISA, register definitions, and extensions. The ████

████ Design allows use of certain features according to the Arm ARM. This

again shows that the ███████ Design (and the Qualcomm Cores which inherited that design) use the Arm Architecture and therefore are ████████ ██████████████████████ How the cores incorporate the architectural features into their microarchitecture is irrelevant and does not change the fact that the ██████████ Design and the Qualcomm Cores from 2021 to 2023 are all Arm-compliant CPUs on a technical level and contain Arm architectural features as identified in my analysis. That the cores have the ability to use Arm ARM features is already a proof of an Arm-based CPU design.

55.   Dr. Annavaram himself states that "development for all of the Qualcomm Cores, other than the ██████████ Core, was started at Qualcomm post-acquisition." (Annavaram Reb. at ¶ 304.) Thus, Qualcomm did inherit the ██████████ Core. Since my analysis principally focuses on the ██████████ Design and the extent to which its RTL was re-used in the later Qualcomm Cores, Dr. Annavaram's focus on components outside the ██████ cores and components Qualcomm may have added post-acquisition are irrelevant. What matters is that, as my analysis shows, ████████████████████████████████████ ██ ██████████████████████████ ██ ███████████████████████████████ ██████████████████████████████████ ████████████████████████████████ ██████████████████████████████████████

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57.   Dr. Annavaram's other arguments are irrelevant. (Annavaram Reb. at¶¶ 304-318.) My understanding is that Arm does not constrain how its customers may optimize their design, such as how/whether they will do clock gating or DFT, etc.   As an example, the designer may choose to perform clock gating for power reduction regardless of the CPU architecture. The point is they use ARM architecture, instructions, and features. The point is that the customers developing a custom Arm-compliant core must use the Arm Architecture, including the instructions and other features. Designers are free to choose specific implementation techniques to further improve the CPU performance and testability, such as various power reduction techniques, Design for Test (DFT), etc.

58.   Dr. Annavaram states that "all the development work on the ███████ Core occurred at Qualcomm under the Qualcomm ALA, and the ████████ Core is targeted to ██████████████████████████." (Annavaram Reb. at ¶¶ 315-18.) I am not a lawyer, and have no opinion on whether work on the ████████ Core was "under the Qualcomm ALA." But, in my opinion, ██████████████████████████████████

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-36-

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59.   Dr. Annavaram's assertion of "[w]ith the exception of several files, none of the files or folders included in Dr. Chen's analysis contained Nuvia-source RTL to be swapped out" (Annavaram Reb. at ¶ 321) confirms that the Swap Out effort ██

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V.   CONCLUSION

60.   My opinions above are based on available information to date. I reserve the right to supplement or amend my opinions in this report, and also to rebut opinions by Qualcomm's experts with which I disagree. I also reserve the right to correct any clerical errors that I discover after service of this report.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct. Executed on this 25th day of March 2024 in Los Angeles, California.

By: _____

     Dr. Shuo-Wei (Mike) Chen

EXHIBIT A
LIST OF MATERIALS CONSIDERED

All documents cited within this report.
Opening Expert Report of Dr. Murali Annavaram and documents referenced therein.
Rebuttal Expert Report of Dr. Murali Annavaram and documents referenced therein.
Opening Expert Report of Dr. Shuo-Wei (Mike) Chen on Confidential Source Code and documents referenced therein.
Opening Expert Report of Dr. Robert P. Colwell and documents referenced therein.
Rebuttal Expert Report of Dr. Robert P. Colwell and documents referenced therein.

PRODUCED MATERIAL
QCARM_2414840
QCARM_2551809
QCARM_2414840

SOURCE CODE PRINTOUTS
QSC1ARMVQC0000101
QSC2ARMVQ0000068-119
QSC2ARMVQ0000120-247

PUBLICLY AVAILABLE SOURCES
Beyond Compare, https://www.scootersoftware.com/v4help/sessiontextalignment.html, (last visited March 24, 2024).
Verilog Examples, https://www.asic-world.com/examples/verilog/index.html, (last visited March 24, 2024).
ARM, https://developer.arm.com/Architectures/A-Profile%20Architecture, (last visited March 24, 2024).

EXHIBIT 19

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

ARM LTD., a U.K. corporation,
        Plaintiff,

     v.

QUALCOMM INC., a Delaware
corporation, QUALCOMM
TECHNOLOGIES, INC., a Delaware
corporation, and NUVIA, INC., a
Delaware corporation,
        Defendants.

C.A. No. 22-1146-MN

**CONTAINS HIGHLY
CONFIDENTIAL – SOURCE
CODE-ATTORNEYS' EYES
ONLY**

**OPENING EXPERT REPORT OF DR. SHUO-WEI (MIKE) CHEN
ON QUALCOMM SOURCE CODE**

ny-2648383

TABLE OF CONTENTS

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I.   INTRODUCTION

1.   My name is Dr. Shuo-Wei (Mike) Chen and I have been retained as an expert witness on behalf of the Plaintiff Arm Ltd. in this matter. I understand that Arm has sued Defendants Qualcomm Inc., Qualcomm Technologies, Inc., and Nuvia, Inc. in the District of Delaware in the case captioned *Arm Ltd. v. Qualcomm Inc. et al.*, No. 1-22-cv-001146-MN (D. Del.). Among other things, I have been asked to review source code produced by Qualcomm and Nuvia in this litigation and analyze (1) similarities between versions of source code and (2) inclusion of various features of Arm's architecture within the source code. I am being compensated for my time in connection with this proceeding at $650/hour. My compensation is not dependent on the substance of my opinions, my testimony, or the outcome of this proceeding.

II.   BACKGROUND

2.   I am a technical expert in digital, analog, and mixed-signal integrated circuit (IC) design. My expertise extends to Register-Transfer Level (RTL) code that is used in digital microprocessors and processors, digital ASICs, and system-on-a-chip (SOC) designs. RTL code, written in Hardware Description Languages (HDLs) like Verilog and VHDL, describe the functionality of hardware components that are ultimately fabricated on devices like processors and SOCs. I have attached my CV as Exhibit A to this report.

3.   I graduated with a Bachelor of Science in Electrical Engineering in 1998 from National Taiwan University, where I was ranked number 1 in the upper division. I received a master's degree in Electrical Engineering and Computer

Science from the University of California, Berkeley in 2002. In 2006, I completed my Ph.D. in Electrical Engineering and Computer Science from the University of California, Berkeley.

4.   I am currently a Professor of Electrical and Computer Engineering at the University of Southern California (USC). My current research involves building electronic circuits and systems that involve intensive digital signal processing, where RTL coding is an essential step for implementing the digital processor on our silicon chips. Prior to USC, I worked in industry for 5 years (2006-2011), building various SOC products that used microprocessors for communications. I have been a professor at USC since 2011.

5.   I have engaged in projects and published papers that involved digital microprocessor/processor design. For example, I worked on an SOC product in industry that I described in a publication in ISSCC 2008 and JSSC 2008, entitled "A Dual-Band CMOS MIMO Radio SoC for IEEE 802.11n Wireless LAN." Another exemplary work involves a digital processor described in an ISSCC 2020 paper, entitled "A 40MHz-BW 76.2dB/78.0dB SNDR/DR noise-shaping nonuniform sampling ADC with single phase-domain level crossing and embedded nonuniform digital signal processor in 28nm CMOS." My work on these projects included writing a significant amount of RTL code.

6.   I have received awards for my work and research. In 2023, I was elevated to IEEE Fellow (class of 2024) in recognition of my technical contributions in solid-state circuit society. In 2022, I was the co-recipient of the ISSCC Jack Kilby

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Award for outstanding achievements in a circuit prototype that leveraged intensive digital signal processing. That same year, I was the co-recipient for the RFIC 2022 Best Student Paper Award for a circuit prototype that also leveraged digital signal processing techniques for a communication system. I was the IEEE Solid-State Circuit Society (SSCS) Distinguished Lecturer from 2021-2023. I have been invited to offer seminars, workshops, keynote talks, and panel discussions in major IEEE conferences, IEEE SSCS chapters, and universities regarding mostly digital circuit architecture for modern integrated circuit design, *i.e.* leveraging digital signal processors for improving the performance and/or reduce cost of the circuit and system.

III.   MATERIALS CONSIDERED

7.   In addition to my personal knowledge and expertise in the field, I have reviewed RTL source code produced by Qualcomm in this case. Based on my review of the source code and correspondence from Qualcomm's counsel (*see* 9/12/2023 email from J. Braly to F. Patel), I understand that Qualcomm produced source code for the following "list of SOCs and cores":

- █████████
    - March 14, 2021
    - February 28, 2022
    - April 1, 2022
    - October 24, 2022
- █████████
    - July 30, 2021

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- o   April 13, 2023

- o   October 24, 2023

- █████████

  - o   January 11, 2022

  - o   July 28, 2023

- █████████ [1] ████

  - o   February 21, 2023

  - o   July 28, 2023

- █████████

  - o   July 28, 2023

8.   I have personally reviewed this source code on a desktop computer

produced by Qualcomm in Los Angeles, CA on the following dates in 2023:

September 15/19/21/22, October 3/4/5/12/13/16/19/20/25/26, November

13/17/20/28/29, and December 1/8/11/12/13/14/15/18. I have spent a total of

approximately 160 hours reviewing source code in this case. I have requested that

Qualcomm produce printed source code and have relied on the requested source

code. Qualcomm has produced printed source code in this case beginning at Bates

No: QSC1ARMVQ0000001 but has not completed producing the printed source code

that I have requested as of my signing of this report.

9.   I have also reviewed various additional materials in forming my

opinions. I reviewed (1) Arm's Complaint filed in this case on August 31, 2022;

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[1] The spelling is from 9/12/2023 email from J. Braly to F. Patel, but the correct spelling appears to be
█████████

(2) the deposition transcripts of Qualcomm witnesses Gerard Williams, Manu Gulati, Nitin Sharma, Jignesh Trivedi, and Pradeep Kanapathipillai; and (3) the deposition transcript of Arm witness Richard Grisenthwaite. Counsel for Arm has provided me with access to all of the deposition transcripts in this litigation, which I have browsed through for background information about the litigation.

10.   I have reviewed the following technical documents produced by Qualcomm and Nuvia:

11.   I have included a list of materials considered as Exhibit B to this report.

IV.   FACTUAL BACKGROUND

12.   Based on my review of the factual materials listed above and public sources, I have the following understanding: Nuvia was founded in early 2019 by

three former Apple employees named Gerard Williams, Manu Gulati, and John

Bruno.[2] Nuvia's goal was to develop a faster and more power-efficient CPU core for

data center applications. The code name for this CPU core was ██████ Nuvia

also developed an SOC called █████ that incorporated the ██████ CPU core.

13.   In December 2020, Nuvia provided a presentation to Qualcomm that

included details about the ██████ core, including the various CPU blocks.

(██.)

14.   On January 21, 2021, Qualcomm announced an agreement to purchase

Nuvia.[3]

15.   On March 15, 2021, Qualcomm announced that it completed its

acquisition of Nuvia.[4]

16.   After the acquisition of Nuvia, the former-Nuvia employees now at

Qualcomm continued to develop the ██████ core. ████████████████

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[2] Stephen Nellis, *Former Apple chip executives found company to take on Intel, AMD*, REUTERS, https://www.reuters.com/article/us-nuvia-tech-idUSKBN1XP19V/?taid=5dcefd5c1dd1a30001b949f0&utm_campaign=trueAnthem%3A+Trending+Content&utm_medium=trueAnthem&utm_source=twitter (last visited December 18, 2023).
[3] QUALCOMM, Press Release: Qualcomm to Acquire NUVIA (Jan. 21, 2021), https://www.qualcomm.com/news/releases/2021/01/qualcomm-acquire-nuvia (last visited December 18, 2023).

[4] QUALCOMM, Press Note: Qualcomm Completes Acquisition of NUVIA (Mar. 15, 2021),https://www.qualcomm.com/news/releases/2021/03/qualcomm-completes-acquisition-nuvia (last visited December 18, 2023).

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██

██████████████ The ████████████████████████████████

(QCARM_3041647) shows the development of ██████ at Qualcomm using a Nuvia

CPU. Similarly, the document entitled "██████████████" states that ██

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(QCARM_0181949 at -950). The "██████████████████████████████████"

document indicates that ████████████████████████████████

██████████████████████ (QCARM_0169739 at -744.)

17.   Qualcomm developed several other SOCs ██████████████

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V.   ANALYSIS AND OPINIONS

A.   Summary of Opinions

18.   I have been asked to perform both quantitative and qualitative

substantive analyses of the RTL code produced by Qualcomm in this case. On the

quantitative side, I have been asked to determine the extent to which source code

developed by Nuvia prior to the Qualcomm acquisition is identical to source code in

7

Qualcomm's products.[5] Based on my analysis, and as further described below, it is my opinion that ██████████████████████

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██ I was also asked to compare the February 28, 2022 ████████ code with the April 1, 2022 ████████ code, and I determined that ██████████████████████

████████

19. On the qualitative side, I have been asked to identify some specific exemplary features of the Arm architecture in the March 14, 2021 ████████ RTL code that are still present in SOCs/cores post-acquisition. Based on my analysis, and as further described below, it is my opinion that the March 14, 2021

████████ RTL code ██████████████████████

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B. Quantitative Approach: RTL Written by Nuvia is Identical in Qualcomm's SOCs/Cores

1. Summary of quantitative approach

20. I performed a quantitative analysis to determine the similarity of source code across different versions of code produced by Qualcomm using the following methodology.

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[5] RTL code is written as text, so I was able to use computer tools to compare text files of RTL code to determine lines of code from versions of the same file that was literally identical to one another.

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21.   First, I relied on the technical documents produced by Qualcomm and Nuvia and the deposition testimony listed in § III to understand some background about Nuvia and Qualcomm's engineering efforts and their nomenclature. I learned that before the Qualcomm acquisition, Nuvia began working on a CPU core ultimately called ███████ ██████ was a custom core that Nuvia designed to implement the Arm architecture and instruction set. Nuvia's design incorporated ██ ████████████ Nuvia further designed an SOC intended for data centers, called ██████ which included ██████████. I also learned that after Qualcomm purchased Nuvia, Qualcomm planned on incorporating the ██████ core into its own SOCs called ████████████████████████. I learned that Qualcomm planned on designing ██████████████████████████.

22.   I also used the technical documentation to identify the design hierarchy of Nuvia's ██████ core and the ██████ I then studied the design directory for the source code produced by Qualcomm. I located the RTL code corresponding to each SOC/core that Qualcomm indicated it had produced: ████████████████ ████████████████████ I found the RTL under: ████████████████████ For example, Qualcomm saved the March 14, 2021 ██████████ code under ██ on the source code desktop.

23.   Under each SOC/core folder, I was able to find the subfolders that corresponded to key building blocks of the SOC/core. For instance, I determined

that the RTL code at the ███████████ was stored under █████

████████████████. I then examined the top-level RTL at the █████████

████ ███████████ and studied the RTL building blocks it instantiates

throughout the design hierarchy. ██████████████████████████

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██████████████████████ By mapping the building blocks across different

code versions, I was able to compare corresponding RTL code between different

SOCs/cores identified by Qualcomm.

24.   I used the March 14, 2021 ████ code as the baseline. ██████████

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████████████████████████████████ I summarize the key

folders in Table 1, below.

25.   The March 14, 2021 ████ code is dated one day before Qualcomm

completed its acquisition of Nuvia. Thus, I understand that the March 14, 2021

████ code reflects the code that Nuvia worked on before the Qualcomm acquisition.

I compared the March 14, 2021 ████ code against all of the other, subsequent

versions of code produced by Qualcomm using a tool called Beyond Compare, which

was installed on the source code desktop. My goal was to assess whether and to

what extent the March 14, 2021 ███████████ code remained the same in the

subsequent code.

26.   I performed this quantitative analysis in two ways in the source code:

(1) identifying key folders and comparing files within those folders across different

SOC/core versions, and (2) identifying top-level RTL files of key building blocks and

comparing each of the RTL files across different SOC/core versions. The results of

both quantitative analyses are the same: ███████████████████████████████

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████████████████

27.   It is noteworthy that I used the default skew tolerance setting in the

Beyond Compare tool. With this default setting, Beyond Compare will search up to

2,000 lines above or below the current line for a matching line during text

alignment. I reserve the right to conduct additional testing with a different skew

tolerance in response to rebuttal arguments by Qualcomm or its experts.

2.   Comparing folder contents across SOC/core versions

28.   As part of my analysis, I identified important source code folders in the

baseline March 14, 2021 ████ code. I mainly focused on the source code folders

related to ██

████████████████ [6] ██

████████████████████████████. In the below table, I identify the folders and

explain the importance of each folder. Some of the CPU block folders contain ██

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[6] ██
██ (*See, e.g.,*
QCARM_2551809████████████████████████████ at -819.)

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Table 1: Key Source Code Folders

29.   Since I was asked to analyze source code related to the ██████ core, there were folders on the source code desktop that I did not consider in my analysis. First, I omitted anything outside of the ████████████████. For instance, I did not consider the ████████████, which contains ████████. Within the ██████ folder, I did not consider ████████████████████████ ██ ████████████████.

30.   For the folders that I did consider, I used the folder comparison function of the Beyond Compare tool to compare the contents of the folders in Table 1 from the March 14, 2021 ████ code to the contents from the same folders in other SOC/core versions produced by Qualcomm. I did two types of analyses.

31.   First, I analyzed the number of common file names within the corresponding folders and calculated the file name similarity (in %). The Beyond

13

Compare tool reports the number of files that do not have common names, so-called "orphan files." I calculated the number of common files names by subtracting the total number of files in the folder by the number of orphan files reported by Beyond Compare. I then calculated the file name similarity (%) as the number of common file names divided by the total number of files in the folder of SOC/core version under comparison.

32.   Second, I analyzed the line similarity (in %) within all the files in the corresponding folders. I used the folder comparison function of the Beyond Compare tool to generate a statistical report (in csv format). The statistical report showed the total number of original, deleted, and changed important/unimportant lines of all the files in the corresponding folder. I then used this spreadsheet to calculate the important line similarity (in %) between the March 14, 2021 Nuvia ███████ code and other SOCs/cores produced by Qualcomm. For any given comparison between two files, the important line similarity (in %) is defined as the number of identical important lines divided by the total number of original important lines. As shown in the tables below, I was able to determine that ██

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██████████████████████████ I have also found the naming

convention of RTL code documented in a technical document, named ██████ ████████ (QCARM_2551809).

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Table 2: Comparing 3/14/2021 ████ Code Folders With ████

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Table 3: Comparing 3/14/2021 ▮▮ Code Folders With ▮▮

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Table 4: Comparing 3/14/2021 ███ **Code Folders With** ██████

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Table 5: Comparing 3/14/2021 ████ Code Folders With ██████

Table 6: Comparing 3/14/2021 ▮▮ Code Folders With ▮▮▮

3. Comparing Key RTL Files Across SOC/core Versions

33.   As part of my analysis, I identified important source code files in the March 14, 2021 ████ code. These files are important because they are the top-level RTL code files in the important design hierarchies and key functional CPU blocks as listed in Table 1. In the table below, I identify the files and explain the specific importance of each file.

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Table 7: Key Source Code Files

34.   I compared these key source code files between the SOC/core version under comparison and the March 14, 2021 ████ code. For this analysis, I used the file comparison function of the Beyond Compare tool, which reports the number of identical lines between two selected files. I then recorded the number of identical lines and calculated the line similarity (in %), defined as the number of identical lines divided by the total number of lines in the RTL file under comparison. Thus,

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for any comparison of two files, the term "line similarity" means the percentage of identical lines of code between the two files. The table below summarizes my analysis.

█	██████ ███	████████ █	███ ██	███████ █	██ ██	███████ █	██ ██
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Table 8: Comparing 3/14/2021 █████ Code Files With ██████

Table 9: Comparing 3/14/2021 ▮▮▮ Code Files With ▮▮▮

Table 10: Comparing 3/14/2021 ▮▮▮ Code Files With ▮▮▮

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Table 11: Comparing 3/14/2021 ██████ Code Files With ██████

Table 12: Comparing 3/14/2021 ██████ Code Files With ██████████

4.   **Comparing February 28, 2022 ▮▮▮▮ code with April 1, 2022 ▮▮▮ code**

35.   I was asked to compare the February 28, 2022 ▮▮▮ code with the

April 1, 2022 ▮▮▮ code to determine the differences between these two versions of

code. I performed this analysis using the same approach that I used to compare

other SOC/core versions (§ V.B.3) except the baseline is now changed to the Feb. 28,

2022 ▮▮▮ code. My conclusion is that the two versions of code are ▮▮▮▮▮▮▮

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Table 13: Comparing 2/28/2022 ▆ Code Folders With 4/1/2022 ▆

Table 14: Comparing 2/28/2022 ▆ Code Files With 4/1/2022 ▆

C. Qualitative Approach: Arm Features are Throughout RTL Code for All SOCs/Cores.

1. Summary of qualitative approach

36. I performed a qualitative analysis to determine what features from the Arm architecture are present in the March 14, 2021 █████ code and are also present in subsequent versions. To perform this analysis, I used the following methodology.

37. First, counsel for Arm identified for me the Arm Architecture Reference Manual v8.7 (G.b) (ARM_01324149) (Arm ARM) and Arm 2020 Architecture Extensions (ARM_00099622). I reviewed those technical documents along with ████████████████████████████ (QCARM_2540979) to identify features/instructions that appear to be specific to Arm. I then used a command-line utility, called grep, to search for and identify those specific features/instructions in the March 14, 2021 █████ code as a baseline. ███████████████████████

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███ I will provide examples in the following sections.

2. ████████████████████████████████

38. ████████████████████████████████ (QCARM_2540979 at -997) ████████████████████████████████████

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opcode is string 0s or 1s that uniquely identify an instruction. ██████████

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    4. █████████████████████████████████████

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50. [REDACTED]

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VI.   CONCLUSION

54.   My opinions above are based on available information to date. I reserve the right to supplement or amend my opinions in this report, and also to rebut opinions by Qualcomm's experts with which I disagree. I also reserve the right to correct any clerical errors that I discover after service of this report.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct. Executed on this 20th day of December of 2023 in Los Angeles, California.

By: _____

     Dr. Shuo-Wei (Mike) Chen

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Exhibit A

Mike Shuo-Wei Chen

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Email: shuowei@gmail.com (Alt: swchen@usc.edu)
Phone: 510-517-0052

Curriculum Vitae

EDUCATION

University of California, Berkeley   2002 – 2006
- PhD in Electrical Engineering and Computer Science
- Dissertation: "High-Speed, Low-Power A/D Converter for a Low-Cost UWB Sub-sampling Radio"
- Advisor: Robert W. Brodersen

University of California, Berkeley   2000 – 2002
- Master of Science in Electrical Engineering and Computer Science
- Thesis: "Ultra Wideband Baseband Design and Implementation"

National Taiwan University   1994 – 1998
- Bachelor of Science in Electrical Engineering
- Top 1 student for upper division

ACADEMIC EXPRIENCE

- Professor, Department of Electrical Engineering, University of Southern California, 2021 – Present.
- Associate Professor, Department of Electrical Engineering, University of Southern California, 2017 – 2021.
- Colleen and Roberto Padovani Early Career Chair, USC, 2014 – 2021
- Assistant Professor, Department of Electrical Engineering, University of Southern California, 2011 – 2017.
- Graduate Student Researcher, Berkeley Wireless Research Center, Berkeley, CA, 2001 – 2006.

WORK EXPRIENCE

- Analog Senior Technical Staff, Atheros Communications, Santa Clara, CA, 2006–2010.
  -Designed RF, analog mixed-signal circuits for various wireless products

CONSULTING EXPERIENCE

- Samsung (2018-now): review their research programs ranging from communication and low power electronic systems

- BAE system (2019-2022): data converter design
- Tetramem (2022-now): AI/ML computing circuitry
- Morrison & Foerster LLP (2019-2022): Xilinx-ADI litigation
    Legal consultant, working with counselors to prepare/review legal documents, non-infringement arguments, deposition, source codes, PTAB, etc.

HONORS and AWARDS

- ISSCC 2022 Jack Kilby Award (co-recipient)
- RFIC 2022 Best Student Paper Award – First Place (co-recipient)
- IEEE Solid-State Circuit Society (SSCS) Distinguished Lecturer 2021-2023.
- DARPA Young Faculty Award (YFA), 2014.
- NSF Faculty Early Career Development (CAREER) Award, 2014.
- Analog Devices Outstanding Student Award, 2006
- UC Regents Fellowship, UC Berkeley, 2000
- Lin's Foundation Award for Top 1 engineering college student over the academic year, 1996-1997
- Presidential Awards, National Taiwan University, 1996-1998
- Member of National Mathematics Team of Taiwan, awarded with Honourable Mention in Asian Pacific Mathematics Olympiad, 1994.

KEY TECHNICAL CONTRIBUTIONS

Analog Mixed-Signal and RF circuit architectures/techniques for data converters, clock generation and PA.

- Asynchronous SAR ADC (since 2006)
- Embedded TDC scheme for Digital PLL (since 2010)
- Nonuniform sampling (NUS) ADCs and NU DSP (since 2012)
- Direct spur/pulling cancellation for Digital PLL (since 2014)
- Dual-rate hybrid DAC (since 2014)
- Sub-harmonic switching (SHS) PA (since 2018)
- Time-Approximation Filter (TAF) for Transceiver (since 2019)
- Two-Point DTC Calibration scheme for Multiplying DLL (since 2021)
- Delay-tracking pipelined SAR TDC (since 2022)

PUBLICATIONS

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2. S. Su*, Q. Zhang*, and **M. S.-W. Chen**, "A 2GS/s 8.5-Bit Time-Based ADC Using a Segmented Stochastic Flash TDC," in 2023 IEEE Custom Integrated Circuits Conference (CICC), Apr. 2023 (* equal contribution)

3. Q. Zhang, H.-C. Cheng, S. Su, and **M. S.-W. Chen**, "A Fractional-N Digital MDLL with Injection Error Scrambling and Background Third-Order DTC Delay Equalizer Achieving –67dBc Fractional Spur," in IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2023. (To appear)

4. Q. Zhang*, S. Su*, and **M. S.-W. Chen**, "A Cost-Efficient Fully Synthesizable Stochastic Time-to-Digital Converter Design Based on Integral Nonlinearity Scrambling," in 2022 59th ACM/EDAC/IEEE Design Automation Conference (DAC), July 2022. (*contributed equally to this work)

5. C. Yang, S. Su and **Mike Chen**, "A Millimeter-Wave Mixer-First Receiver with Non-Uniform Time-Approximation Filter Achieving >45-dB Blocker Rejection," in IEEE Radio Frequency Integrated Circuits Symposium (RFIC), June 2022. (Best Student Paper Award – First Place)

6. S. Su, and **M. S.-W. Chen**, "High-Speed Digital-to-Analog Converter Design Towards High Dynamic Range," (invited paper) *IEEE Custom Integrated Circuits Conference (CICC), Apr. 2022.*

7. J. Liu, M. Hassanpourghadi, and **M. S.-W. Chen**, "A 10GS/s 8b 25fJ/c-s 2850um2 Two-Step Time-domain ADC Using Delay-Tracking Pipelined-SAR TDC with 500fs Time Step in 14nm CMOS Technology", *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2022.

8. S. Su, Q. Zhang, M. Hassanpourghadi, J. Liu, R.A. Rasul, and **M. S.-W. Chen**, "Analog/Mixed-Signal Circuit Synthesis Enabled by the Advancements of Circuit Architectures and Machine Learning Algorithms," (invited paper) *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2022.

9. S. Su, Q. Zhang, J. Liu, M. Hassanpourghadi, R.A. Rasul, and **M. S.-W. Chen**, "TAFA: Design Automation of Analog Mixed-Signal FIR Filters Using Time Approximation Architecture," *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2022.

10. J. Liu, S. Su, M. Madhusudan, M. HHassanpourghadi, S. Saunders, Q. Zhang, R. Rasul, Y. Li, J. Hu, A. Kumar, S. S. Sapatnekar, R. Harjani, A. Levi, S. Gupta and **M. S.-W. Chen**, "From Specification to Silicon: Towards Analog/Mixed-Signal Design Automation using Surrogate NN Models with Transfer Learning", *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 2021.

11. M. Hassanpourghadi, S. Su, R.A. Rasul, J. Liu, Q. Zhang, and **M. S.-W. Chen**, "Circuit Connectivity Inspired Neural Network for Analog Mixed-Signal Functional Modeling," *58th ACM/EDAC/IEEE Design Automation Conference (DAC)*, Dec. 2021.(to appear)

12. R.A. Rasul, and **M. S.-W. Chen**, "A 128×128 SRAM Macro with Embedded Matrix-Vector Multiplication Exploiting Passive Gain via MOS Capacitor for Machine Learning Application," *IEEE Custom Integrated Circuits Conference (CICC), Apr. 2021.*

13. A. Zhang, M. Ayesh, S. Mahapatra, and **M. S.-W. Chen**, "A 24-28 GHz Concurrent Harmonic and Subharmonic Tuning Class E/F2,2/3 Subharmonic Switching Power Amplifier Achieving Peak/PBO Efficiency Enhancement," *IEEE Custom Integrated Circuits Conference (CICC), Apr. 2021.*

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14. Q. Zhang, S. Su, C.-R. Ho, and **M. S.-W. Chen**, "A Fractional-N Digital MDLL with Background Two-Point DTC Calibration Achieving -60dBc Fractional Spur," *IEEE International Solid-State Circuits Conference (ISSCC),* Feb. 2021.

15. A. Zhang, C. Yang, M. Ayesh, and **M. S.-W. Chen**, "A 5-6 GHz Current-Mode Subharmonic Switching Digital Power Amplifier for Enhancing Power Back-off Efficiency," *IEEE International Solid-State Circuits Conference (ISSCC),* Feb. 2021.

16. Q. Zhang, S. Su, J. Liu and **M. S.-W. Chen**, "CEPA: CNN-based Early Performance Assertion Scheme for Analog and Mixed-Signal Circuit Simulation," in *2020 IEEE/ACM International Conference on Computer-Aided Design (ICCAD),* November 2020.

17. J. Liu, M. Hassanpourghadi, Q. Zhang, S. Su and **M.S.-W. Chen**, "Transfer Learning with Bayesian Optimization-Aided Sampling for Efficient AMS Circuit Modeling," in *2020 IEEE/ACM International Conference on Computer-Aided Design (ICCAD),* November 2020.

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19. S. Su and **M. S.-W. Chen**, "A SAW-Less Direct-Digital RF Modulator with Tri-Level Time-Approximation Filter and Reconfigurable Dual-Band Delta-Sigma Modulation," *IEEE International Solid-State Circuits Conference (ISSCC),* Feb. 2020.

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23. M. Hassanpourghadi, **M.S-W Chen**, "A 2-way 7.3-bit 10 GS/s Time-based Folding ADC with Passive Pulse-Shrinking Cells," *IEEE Custom Integrated Circuits Conference (CICC)*, April 2019.

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32. J.W. Nam, M. Hassanpourghadi, A. Zhang, **M.S-W Chen**, "A 12-bit 1.6 GS/s Interleaved SAR ADC with Dual Reference Shifting and Interpolation Achieving 17.8 fJ/conv-step in 65nm CMOS," *IEEE Symposia on VLSI Technology and Circuits (VLSIC),* June 2016.

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42. **M. S.W. Chen**, "Overhead Minimization Techniques for Digital Phase-Locked Loop Frequency Synthesizer, " IEEE MWSCAS (Invited Session), Aug. 2012.

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45. A. Fort, **M. S.-W. Chen**, R.W. Brodersen, C. Desset, P. Wambacq, <u>L. Van Biesen</u>, "Impact of Sampling Jitter on Mostly-Digital Architectures for UWB Bio-Medical Applications," *IEEE International Conference on Communications (ICC)*, June 2007.

46. A. Fort, **M. S.-W. Chen**, C. Desset, P. Wambacq, <u>L. Van Biesen</u>, "Clock offset tracking for subsampling UWB architectures in a body area network," *IEEE International Conference on Ultra-Wideband (ICUWB)*, Sep. 2007.

47. **M. S.-W. Chen** and R. W. Brodersen, "Digital Complex Signal Processing Techniques for Impulse Radio," *Global Telecommunications Conference (GLOBECOM)*, Nov. 2006.

48. **M. S.-W. Chen** and R. W. Brodersen, "Implementation Considerations for a Sub-sampling Impulse Radio," *IEEE International Conference on Ultra-Wideband (ICUWB)*, Sep. 2006.

49. **M. S.-W. Chen** and R. W. Brodersen, "A 6b 600MS/s 5.3mW Asynchronous ADC in 0.13μm CMOS," *IEEE International Solid-State Circuits Conference (ISSCC),* Feb. 2006.

50. D. Cabric, **M. S.-W. Chen**, D. Sobel, J. Yang, and R. Brodersen, "Future Wireless Systems: UWB, 60 GHz, and Cognitive Radios," (Invited paper) at *Custom Integrated Circuits Conference (CICC)*, Sep. 2005

51. **M. S.-W. Chen**, R. W. Brodersen, "The Impact of a Wideband Channel on UWB System Design," *Military Communication Conference (MILCOM)*, Nov. 2004.

52. **M. S.-W. Chen**, R. W. Brodersen, "A Subsampling UWB Radio Architecture by Analytic Signaling," *International Conference on Acoustics, Speech, and Signal Processing (ICASSP)*, May 2004.

53. I. O'Donnell, **M. S.-W. Chen**, S. Wang, R. W. Brodersen, "An Integrated, Low-Power, Ultra-Wideband Transceiver Architecture for Low-Rate, Indoor Wireless Systems," *IEEE CAS Workshop on Wireless Communications and Networking*, Sep. 2002.

Journals

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1. C. Yang, S. Su, and M. S.-W. Chen, "Millimeter-Wave Receiver with Non-Uniform Time-Approximation Filter," IEEE J. Solid-State Circuits, 2023 (in press).
2. J. Liu, M. Hassanpourghadi, and M. S.-W. Chen, "A 10-GS/s 8-bit 2850-μm2 Two-Step Time-Domain ADC With Speed and Efficiency Enhanced by the Delay-Tracking Pipelined-SAR TDC," IEEE J. Solid-State Circuits, 2022.
3. S. Su and **M. S.-W. Chen**, "SAW-Less Direct RF Transmitter with Multi-Mode Noise Shaping and Tri-Level Time-Approximation Filter," IEEE J. Solid-State Circuits, Mar. 2022.
4. Q. Zhang, S. Su, C.-R. Ho, and **M. S.-W. Chen**, "A Fractional-N Digital MDLL With Background Two-Point DTC Calibration," (Invited) *IEEE J. Solid-State Circuits* (JSSC), Jan. 2022.
5. M. Hassanpourghadi, R. A. Rasul, and **M. S. W. Chen**, "A Module-Linking Graph Assisted Hybrid Optimization Framework for Custom Analog and Mixed-Signal Circuit Parameter Synthesis" ACM Transactions on Design Automation of Electronic Systems, June 2021.
6. X. Yan, J. Ma, T. Wu, A. Zhang, J. -B. Wu, M. Chin, Z. Zhang, M. Dubey, W. Wu, **M. S.-W. Chen**, J. Guo, H. Wang "Reconfigurable Stochastic Neurons Based on Tin Oxide/MoS2 Hetero-memristors for Simulated Annealing and the Boltzmann Machine" Nature Communications, 12, Article number: 5710 (2021)
7. S. Su, **M. S.-W. Chen**, "A Time-approximation Filter for Direct RF Transmitter," *IEEE J. Solid-State Circuits* (JSSC) 2021.
8. J.W. Nam, **M. S.-W. Chen**, "A 12.8-Gbaud ADC-based Wireline Receiver with Embedded IIR Equalizer," (Invited) *IEEE J. Solid-State Circuits* (JSSC), Mar. 2020.
9. A. Zhang, **M. S-W. Chen**, "A Watt-Level Phase-Interleaved Multi-Subharmonic Switching Digital Power Amplifier," (Invited) *IEEE J. Solid-State Circuits* (JSSC) Nov., 2019.
10. A. Zhang, **M. S-W. Chen**, "A Subharmonic Switching Digital Power Amplifier for Power Back-Off Efficiency Enhancement," (Invited) *IEEE J. Solid-State Circuits* (JSSC) Feb., 2019.
11. T.F. Wu, **M. S.-W. Chen**, "A VCO-Based Nonuniform Sampling ADC with Phase-Domain Level Crossing," (Invited) *IEEE J. Solid-State Circuits* (JSSC) Mar., 2019.
12. S. Su, **M. S.-W. Chen**, "A 16-bit 12GS/s Single/Dual-Rate DAC with a Successive Bandpass Delta-Sigma Modulator Achieving <-67dBc IM3 within DC to 6GHz Tunable Passbands," (Invited) *IEEE J. Solid-State Circuits* (JSSC) Dec., 2018.
13. T.F. Wu, **M. S-W. Chen**, "A Subranging-Based Nonuniform Sampling ADC With Sampling Event Filtering," *IEEE Solid-State Circuits Letters* (SSC-L) April, 2018.
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INVITED TALKS/TUTORIALS/WORKSHOPS

1. ITRI, Taiwan, "New Opportunities in Mixed-Signal ICs", June, 2011.
2. UMC, Taiwan, "New Opportunities in Mixed-Signal ICs", June, 2011.
3. HRL Laboratories, LLC: "Enhancing A-to-D Conversion Efficiency". July 2nd, 2012

Mike Shuo-Wei Chen

4. "Analog-to-Digital Interface: A Time Approach" 2013 CMOS Emerging Technologies Research Symposium, Whistler, July 2013.
5. "Path towards High-Speed High-Resolution Data Converters with Diminishing Cost", Sep. 2013, Broadcom.
6. "Analog-Digital Interface Research, really?" Sep. 2013, Qualcomm-Atheros.
7. "Re-shape Future Mixed-Signal IC Design" Oct. 2013. Qualcomm.
8. "Path towards High-Speed High-Resolution Data Converters with Diminishing Cost", Nov. 2013, UT Dallas.
9. "Path towards High-Speed High-Resolution Data Converters with Diminishing Cost", Nov. 2013, Texas Instrument.
10. "Power efficient ADC Topologies towards RF Sampling" 2014 RFIC Tutorial.
11. "Path Towards Direct RF Synthesis: A Hybrid Digital-to-Analog Converter Architecture" 2014 IEEE MWSCAS Conference, Distinguished Speaker Series.
12. "Asynchronous SAR ADC: Past, Present and Beyond" 2014 IEEE MWSCAS Conference Tutorial
13. "Exploring Limits of Mixed-Signal ICs" Sep. 2014, MaxLinear Corp.
14. "Rethinking Analog-Digital Interface Circuit Architectures" Oct. 2014, IC Seminar, Columbia University, NY.
15. "Rethinking Analog-Digital Interface Circuit Architectures" Mar. 2015, IC Seminar, UC Berkeley, CA.
16. "Rethinking Analog-Digital Interface Circuit Architectures" Dec. 2015, IC Seminar, National Taiwan University(NTU)/IEEE Chapter, Taipei, Taiwan.
17. "Rethinking Analog-Digital Interface Circuit Architectures" Feb. 2016, IC Seminar, UT Austin, Texas.
18. "Asynchronous SAR ADC: Past, Present and Beyond", Feb. 2016, EE department Colloquium, UT Austin/IEEE Chapter.
19. "Rethinking Analog-Digital Interface Circuit Architectures" Feb. 2016, IC Seminar, University of Michigan, Ann Arbor.
20. "Rethinking Analog-Digital Boundary from Circuit to System Level towards Reconfigurability of Everything" Mar. 2016, SystemX Seminar, Stanford
21. "Rethinking Analog-Digital Interface Circuit Architectures" April. 2016, EE department Colloquium. Carnegie Mellon University (CMU).
22. "Rethinking Analog-Digital Interface Circuit Architectures" April. 2016, IC Seminar, University of California, Los Angeles (UCLA).
23. "IC Research overview," TSMC, 2017
24. "IC Research overview," Intel Lab, 2017
25. "IC Research overview," InPhi, 2017
26. "Advancing Low-Power High-Speed Analog-to-Digital Converters: An Asynchronous Design Approach", VLSI DAT tutorial, 2017
27. "Generic spur cancellation for digital PLL," Qualcomm 2017
28. "Evolutions of SAR ADC: from High Resolution to High Speed Regime," IEEE CICC 2018 tutorial.
29. "Emerging Opportunities in Analog Mixed-Signal Circuit Design Automation," ACM/IEEE ICCAD 2018 workshop.
30. "Analog-to-Digital Converter Architecture Opportunities in Emerging Wireless Systems," RFIC 2018 workshop

31. "How can hardware designers reclaim the spotlight?" moderator/co-organizer of ISSCC 2019 evening panel.
32. "Fundamentals of Analog-to-digital conversion," 2-day tutorial in Shanghai, China 2019.
33. "Digital Fractional-N Phase Locked Loop Design," tutorial, ISSCC Feb 2020
34. "Digital Fractional-N Phase Locked Loop Design," ISSCCedu Feb 2020
35. "Low Spur PLL architectures," MEAD tutorial in EPFL, 2021 (to appear)
36. "Low Spur PLL architectures and techniques, " IEEE CICC 2020
37. "New Opportunities in Nonuniform Sampling," IEEE SSCS Webinar Oct 2020.
38. "High-Performance Digital-to-Analog Converter Design: A Path towards Digital Transmitter," ISESD Keynote June 2021
39. "ADC Evolution via Architectural Rethinking: from Asynchronous SAR to Non-uniform Sampling ADC," IEEE SSCS Tainan Chapter, Oct 2021
40. "High-Performance Digital-to-Analog Converter Design: A Path towards Digital Transmitter," IEEE SSCS Atlanta Chapter, Nov. 2021
41. "Asynchronous SAR ADC: Past, Present and Beyond," IEEE Southern Alberta Chapter, Nov. 2021
42. "Non-Uniform Sampling Data Converters: A Journey to Uncharted Circuits and Systems" IEEE VLSI-DAT April 2022
43. "Asynchronous SAR ADC: Past, Present and Beyond," IEEE Swiss Chapter, May 2022
44. "New Opportunities in Nonuniform Sampling," IEEE Penang Chapter, July 2022
45. "Trend in Digital PLL Design and New Opportunities in Spur Cancellation," IEEE Southern Alberta Chapter, Sep. 2022
46. "High-Performance Digital-to-Analog Converter Design: A Path towards Digital Transmitter," IEEE Egypt Chapter Nov. 2022
47. "New Opportunities in Nonuniform Sampling," IEEE Taipei Chapter, Dec. 2022
48. "Trend in Digital PLL Design and New Opportunities in Spur Cancellation," IEEE Tainan Chapter, Dec. 2022

PROFESSIONAL SERVICES

Review Panel:
1. IEEE SSCS James D. Meindl Innovators Award
2. NSF Panelist
3. Samsung Research

Journal article review:
1. IEEE Journal of Solid-State Circuits
2. IEEE Solid-State Circuits Letters (SSC-L)
3. IEEE Transactions on Signal Processing
4. IEEE Transactions on Communications
5. IEEE Transactions on Circuits and Systems I
6. IEEE Transactions on Circuits and Systems II
7. IEEE Transactions on Vehicular Technology
8. IEEE Communications Letters

Mike Shuo-Wei Chen

    9. Journal of VLSI Signal Processing Systems

USC Department Services:
1. Munishian Series Committee
2. EFC
3. EE Festival reviewer

Conference TPC:
IEEE European Conference on Solid-State Circuits (ESSCIRC) (2022- present)
IEEE International Solid State Circuits Conference (ISSCC) (2018 - present)
IEEE Symposium on VLSI Circuits (VLSIC) (2017 - 2020)
IEEE Custom Integrated Circuits Conference (CICC) (2015 - 2019)
IEEE GlobalSIP (2014)

Organized/Participated Panel/Forum/Workshops for SSCS:
1. Forum: "Emerging Design Techniques for Data Converters" served as organizer at CICC 2017
2. Panel: "What can/should Circuit Designers do to Ride on the Wave of Machine Learning?" served as co-organizer and moderator at CICC 2018
3. Panel: "How can hardware designers reclaim the spotlight?" served as co-organizer and moderator at ISSCC 2019
4. Panel: "Favorite circuit design and testing mistakes of starting engineers?" served as co-organizer at ISSCC 2021
5. VLSI Symposia Mentoring Event June 2021
6. Panel: "How to choose career path, academia, industry, startups?" served as panelist at CICC 2022 (to appear)
7. Panel: "Open Source Systems, Circuits, and Design: Is It the Future?" served as panelist at CICC 2022 (to appear)

Associate Editor:
SSC-L, TCAS-II

Society Membership:
Senior Member of IEEE

CURRENT, PRIOR, AND PENDING RESEARCH GRANTS

Current Research Grants

Proposal Title: SpecEES: Switched-Capacitor Radiofrequency Signal Processing for Spectrally-Agile Low-Energy Wireless Transceivers
Source of Support: NSF: ECCS-1824442
Project Location: USC PI: Hossein Hashemi, Co-PI: Mike Chen
Total Award Amount: $675,000 (Chen's share: $313,991)
Starting Date: 09/01/2018   Ending Date: 08/31/2023

Mike Shuo-Wei Chen

Proposal Title: Bio-inspired hybrid computing platform for micro-unmanned vehicles
Source of Support: IARPA: 2021-21090200005
Project Location: USC PI: Wei Wu, Co-PIs: Mike Chen, Quan Nguyen
Total Award Amount: $3,000,000 (Chen's share: $1,100,000)
Starting Date: 09/27/2021   Ending Date: 10/26/2023

Proposal Title: High-Speed Multi-GS/s Time-based ADC
Source of Support: MediaTek Inc.
Project Location: USC PI: Mike Chen
Total Award Amount: $160,000
Starting Date: 01/01/2022   Ending Date: 01/01/2024

Proposal Title: Center for Ubiquitous Connectivity (CUbiC)
Source of Support: Columbia University (Prime: SRC): 2023-JU-3132
Project Location: USC PI: Mike Chen
Total Award Amount: $1,250,000
Starting Date: 01/01/2023   Ending Date: 12/31/2027

Proposal Title: High-Speed DAC with High Output Power and Linearity
Source of Support: University of Texas at Dallas (Prime: SRC): 2023-AM-3160
Project Location: USC PI: Mike Chen
Total Award Amount: $270,000
Starting Date: 01/01/2023   Ending Date: 12/31/2025

Proposal Title: Machine-Learning Based Analog Mixed-signal Design Tool
Source of Support: University of Texas at Dallas (Prime: SRC): 2023-AM-3160
Project Location: USC PI: Mike Chen, Co-PIs: Sandeep Gupta, Anthony Levi
Total Award Amount: $285,000 (Chen's share: $259,568)
Starting Date: 01/01/2023   Ending Date: 12/31/2025

Proposal Title: Design Automation of Low Phase Noise PLL
Source of Support: University of Texas at Dallas (Prime: SRC): 2023-AM-3160
Project Location: USC PI: Mike Chen, Co-PIs: Sandeep Gupta, Anthony Levi
Total Award Amount: $270,000 (Chen's share: $244,568)
Starting Date: 01/01/2023   Ending Date: 12/31/2025

Prior Research Grants

Proposal Title: Techniques Estimating Reliability in COTS ICs (Phase 1)
Source of Support: DARPA: HR0011-11-C-0067 CLIN0001
Project Location: USC PI: Michael Fritze, Co-PI: Mike Chen
Total Award Amount: $2,428,225 (Chen's share: $299,153)

Mike Shuo-Wei Chen

Starting Date: 07/21/2011   Ending Date: 03/07/2013

Proposal Title: Techniques Estimating Reliability in COTS ICs (Phase 2)
Source of Support: DARPA: HR0011-11-C-0067 CLIN0002
Project Location: USC PI: Michael Fritze, Co-PI: Mike Chen
Total Award Amount: $1,787,093 (Chen's share: $47,783)
Starting Date: 02/20/2013   Ending Date: 09/20/2014

Proposal Title: Silicon-Based Monolithic Digital RF Memory
Source of Support: ONR: N00014-11-1-0819
Project Location: USC PI: Hossein Hashemi, Co-PI: Mike Chen
Total Award Amount: $1,200,000 (Chen's share: $600,000)
Starting Date: 08/01/2011   Ending Date: 09/30/2015

Proposal Title: Multi-Tier Reconfigurable Transceivers for Hand-Portable Radio and
                      Micro Base Stations
Source of Support: DARPA: HR0011-12-C-0094
Project Location: USC PI: Hossein Hashemi, Co-PI: Mike Chen
Total Award Amount: $3,257,252 (Chen's share: $400,000)
Starting Date: 08/20/2012   Ending Date: 07/15/2017

Proposal Title: Computational Leverage Against Surveillance Systems (CLASS)
Source of Support: Itt Exelis (Prime: DARPA): 473685J
Project Location: USC PI: Mike Chen
Total Award Amount: $287,125
Starting Date: 06/12/2013   Ending Date: 12/22/2014

Proposal Title: Design of Integrated Circuit for Intravascular Radial Arrays
Source of Support: Texas Instruments Inc.
Project Location: PI: K. Kirk Shung, Co-PI: Mike Chen
Total Award Amount: $150,000 (Chen's share: $29,332)
Starting Date: 02/01/2014   Ending Date: 01/31/2015

Proposal Title: Dual-Channel UWB Impulse-Based Interconnect Towards Large-Scale
                      Plastic Neural Network
Source of Support: DARPA YFA (SPANAVWAR): N66001-14-1-4049
Project Location: USC PI: Mike Chen
Total Award Amount: $500,000
Starting Date: 09/04/2014   Ending Date: 09/03/2017

Proposal Title: Computational Leverage Against Surveillance Systems (CLASS) Phase 2

Mike Shuo-Wei Chen

Source of Support: NexGen (Prime: DARPA): 004897-00001
Project Location: USC PI: Mike Chen
Total Award Amount: $450,000
Starting Date: 10/01/2014   Ending Date: 03/31/2016

Proposal Title: R2 Transceiver Integration
Source of Support: Google: R2-USC-01
Project Location: USC PI: Mike Chen
Total Award Amount: $800,000
Starting Date: 04/23/2015   Ending Date: 03/31/2016

Proposal Title: R2 2.0 Transceiver Integration - 2016 (Statement of Work #R2-USC-02)
Source of Support: Google: 349783
Project Location: USC PI: Mike Chen
Total Award Amount: $600,000
Starting Date: 04/01/2016   Ending Date: 12/31/2016

Proposal Title: Wideband High-Dynamic Arbitrary Signal Generator for Electronic
                      Warfare Integrated Systems Research
Source of Support: ONR (DURIP): N00014-15-1-2817
Project Location: USC PI: Hossein Hashemi, Co-PI: Mike Chen
Total Award Amount: $189,500
Starting Date: 09/29/2015   Ending Date: 09/27/2017

Proposal Title: Calibration and Characterization of High-Speed Data Converter and Clock
                      Generator
Source of Support: ONR: N00014-15-1-2864
Project Location: USC PI: Hossein Hashemi, Co-PI: Mike Chen
Total Award Amount: $150,000 (Chen's share: $100,383)
Starting Date: 09/30/2015   Ending Date: 06/30/2016

Proposal Title: Support for April 2017 Connectivity CDF
Source of Support: Airbus: SWLA00034
Project Location: USC PI: Mike Chen
Total Award Amount: $20,000
Starting Date: 04/26/2017   Ending Date: 05/31/2017

Proposal Title: CAREER: Asynchronous Analog-to-Digital Converters with Non-
                      Uniform Discrete-Time Signal Processing
Source of Support: NSF: ECCS-1351956
Project Location: USC PI: Mike Chen
Total Award Amount: $400,000

Mike Shuo-Wei Chen

Starting Date: 02/15/2014   Ending Date: 01/31/2020

Proposal Title: EARS: Enabling Opportunistic Environmental Monitoring with Non-
                       Uniform Sampling and Processing Circuits
Source of Support: NSF: ECCS-1643004
Project Location: USC PI: Mike Chen, Co-PIs: Mahta Moghaddam, Keith Chugg
Total Award Amount: $899,998 (Chen's share: $300,000)
Starting Date: 10/01/2016   Ending Date: 09/30/2021

Proposal Title: Automated Analog Mixed-Signals (AMS) Intellectual Property Generator
                       for Complementary Metal Oxide Semiconductor (CMOS) Technologies
Source of Support: DARPA (account managed by AFRL): FA8650-18-2-7853
Project Location: USC PI: Anthony Levi, Co-PIs: Mike Chen, Sandeep Gupta, Wes Hanford
Total Award Amount: $6,028,731 (Chen's share: $ $1,930,468)
Starting Date: 06/25/2018   Ending Date: 12/30/2022

Proposal Title: Discrete-time mm-wave Processors for Scalable Digital Arrays
Source of Support: DARPA (account managed by AFRL): FA8650-19-1-7996
Project Location: USC PI: Hossein Hashemi, Co-PI: Mike Chen
Total Award Amount: $1,200,000 (Chen's share: $600,000)
Starting Date: 10/09/2018   Ending Date: 01/10/2023

Pending Research Grants

Proposal Title: CMOS Integrated Warm Electronics for Large Format Far Infrared
                       Detectors
Source of Support: Jet Propulsion Laboratory (Prime: NASA)
Project Location: USC PI: Mike Chen
Total Award Amount: $393,294
Starting Date: 10/01/2023   Ending Date: 09/30/2026

Proposal Title: SHF: Medium: Transistors to Algorithm Hardware Acceleration of
                       Boolean Satisfiability (SAT) and NP Complete Problems
Source of Support: NSF
Project Location: USC PI: Sandeep Gupta, Co-PIs: Pierluigi Nuzzo, Mike Chen, Tony Levi
Total Award Amount: $1,199,994 (Chen's share: $259,544)
Starting Date: 10/01/2023   Ending Date: 09/30/2026

Proposal Title: ACED Fab: 3D memristor/CMOS Hybrid Field-programmable Analog
                       Arrays for Signal Processing from RF to Baseband
Source of Support: NSF
Project Location: USC PI: Mike Chen, Co-PIs: Joshua Yang, Qiangfei Xia

Mike Shuo-Wei Chen

Total Award Amount: $600,000 (Chen's share: $420,000)
Starting Date: 07/01/2023   Ending Date: 06/30/2026

Proposal Title: EFRI BRAID: Efficient learning in strongly-biased memristor-based
                      neural architectures
Source of Support: NSF
Project Location: USC PI: Bartlett Mel, Co-PIs: Joshua Yang, Mike Chen, Greg Ver Steeg
Total Award Amount: $1,996,702 (Chen's share: $94,202)
Starting Date: 08/16/2023   Ending Date: 08/15/2027

Exhibit B
List of Materials Considered

All documents cited within this report.
Qualcomm Source Code computer.

Source Code

All source code print requests submitted by Dr. Chen, including:
- QSC1ARMVQC0000001 – QSC1ARMVQC0000021
- QSC1ARMVQC0000022 – QSC1ARMVQC0000064
- QSC1ARMVQC0000065 – QSC1ARMVQC0000145
- QSC1ARMVQC0000146 – QSC1ARMVQC0000188
- QSC1ARMVQC0000189 – QSC1ARMVQC0000259
- Any print outs requested by Chen and not yet provided by Qualcomm at the time of signing this report.

Correspondences

- Correspondence dated 09/12/2023, email from J. Braly to F. Patel

Pleadings

- Arm Ltd. v. Qualcomm Inc. et al., No. 1-22-cv-001146 MN (D. Del.):
  ECF No. 1, Complaint, dated August 31, 2022.

Discovery

- Defendants' Response and Objections to Plaintiff's First Set of Interrogatories (Nos. 1-13), dated February 27, 2023.
- Plaintiff's Third Set of Requests for Production to Defendants (Nos. 59-122), dated July 19, 2023.

Deposition Transcripts

Singh Deposition Transcript dated September 22, 2023.
Gulati Deposition Transcript dated October 12, 2023.
Chunduru Deposition Transcript dated October 20, 2023.
Herbert Deposition Transcript dated October 25, 2023.
Trivedi Deposition Transcript dated October 25, 2023.
Abbey Deposition Transcript dated October 27, 2023.
Sharma Deposition Transcript dated October 27, 2023.
Couillard Deposition Transcript dated November 2, 2023.
Williams Deposition Transcript dated November 3, 2023.
Asghar Deposition Transcript dated November 8, 2023.

Williamson Deposition Transcript dated November 9, 2023.
Amon Deposition Transcript dated November 15, 2023.
Grisenthwaite Deposition Transcript dated November 15, 2023.
Segars Deposition Transcript dated November 16, 2023.
Roberts Deposition Transcript dated November 28, 2023.
Thompson Deposition Transcript dated November 28, 2023.
Bos Deposition Transcript dated November 29, 2023.
Shivashankar Deposition Transcript dated November 30, 2023.
Kanapathipillai Deposition Transcript dated December 1, 2023.
Werkheiser Deposition Transcript dated December 7, 2023.
Armstrong Deposition Transcript dated December 8, 2023.
Balakrishnan Deposition Transcript dated December 8, 2023
Haas Deposition Transcript dated December 12, 2023.
Sands Deposition Transcript dated December 14, 2023.

Websites

- Stephen Nellis, *Former Apple chip executives found company to take on Intel, AMD*, REUTERS, https://www.reuters.com/article/us-nuvia-tech-idUSKBN1XP19V/?taid=5dcefd5c1dd1a30001b949f0&utm_campaign=trueAnthem%3A+Trending+Content&utm_medium=trueAnthem&utm_source=twitter (last visited December 18, 2023).
- QUALCOMM, Press Release: Qualcomm to Acquire NUVIA (Jan. 21, 2021), https://www.qualcomm.com/news/releases/2021/01/qualcomm-acquire-nuvia (last visited December 18, 2023).
- QUALCOMM, Press Note: Qualcomm Completes Acquisition of NUVIA (Mar. 15, 2021), https://www.qualcomm.com/news/releases/2021/03/qualcomm-completes-acquisition-nuvia (last visited December 18, 2023).

Produced Documents

ARM_00099622 (NUVIA248705)	ARM_01324149	QCARM_0000864	QCARM_0169739
QCARM_0170271	QCARM_0181939	QCARM_0181947	QCARM_0181949
QCARM_0325086	QCARM_0325371	QCARM_0332617	QCARM_0359951
QCARM_0490031	QCARM_0490329	QCARM_2396579	QCARM_2402257
QCARM_2402586	QCARM_2412688	QCARM_2414840	QCARM_2540979
QCARM_2551809	QCARM_3041647	QCARM_3087396	QCARM_3087757
QCARM_3087992	QCARM_3088245	QCARM_3088553	QCARM_3088937
QCARM_3089361			

EXHIBIT 20

Page 1

1   IN THE UNITED STATES DISTRICT COURT

2   FOR THE DISTRICT OF DELAWARE

3

     ARM LTD.,   )

4   )

             PLAINTIFF,   )

5   )

             VS.   ) Case No. 22-1146 (MN)

6   )

     QUALCOMM INC., QUALCOMM   )

7   TECHNOLOGIES, INC., and   )

     NUVIA, INC.,   )

8   )

             DEFENDANTS.   )

9   _____)

10

11

12   VIDEOTAPED DEPOSITION OF DR. SHUO-WEI (MIKE) CHEN

13   TRANSCRIPT MARKED HIGHLY CONFIDENTIAL

14   TUESDAY, JUNE 25, 2024, 9:12 A.M.

15   LOS ANGELES, CALIFORNIA

16

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23   Reported by Desiree Cooks, CSR No. 14075

24   Job No. 6768176

25   Pages 1 - 188

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1 IN THE UNITED STATES DISTRICT COURT
2 FOR THE DISTRICT OF DELAWARE
3
4
   ARM LTD.,   )
5   )
       PLAINTIFF,   )
6   )
       VS.   ) Case No. 22-1146 (MN)
7   )
   QUALCOMM INC., QUALCOMM   )
8 TECHNOLOGIES, INC., and   )
   NUVIA, INC.,   )
9   )
       DEFENDANTS.   )
10 _____)
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20
21 THE VIDEOTAPED DEPOSITION OF DR. SHUO-WEI (MIKE) CHEN,
22 taken at 707 Wilshire Boulevard, 60th Floor, Los Angeles,
23 California, on Tuesday, June 25, 2024, at 9:12 a.m.,
24 before Desiree Cooks, Certified Shorthand Reporter, in
25 and for the State of California.

Page 3

1 APPEARANCES:
2 For the Plaintiff:
3   MORRISON & FOERSTER LLP
     BY: NICHOLAS FUNG, ESQ.
4   707 Wilshire Boulevard, 60th Floor
     Los Angeles, California 90017
5   (650) 813-5688
     Nfung@mofo.com
6
7 For the Defendants:
8   PAUL WEISS RIFKIND WHARTON & GARRISON, LLP
     BY: CATHERINE NYARADY, ESQ.
9   -- JACOB BRALY, ESQ.
     1285 Avenue of the Americas
10   New York, New York 10019
     (212) 492-0726
11   Cnyarady@paulweiss.com
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12
     NORTON ROSE FULBRIGHT, LLP
13   BY: JOHN POULOS, ESQ.
     1045 West Fulton Street, Suite 1200,
14   Chicago, Illinois 60607
     (312) 964-7766
15   John.poulos@nortonrosefulbright.com
16
   Also present:
17
     Jacob Florez, Videographer
18
19
20
21
22
23
24
25

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2
3 WITNESS: DR. SHUO-WEI (MIKE) CHEN
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5 EXAMINATION   PAGE
6 BY MS. NYARADY   7
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10   INFORMATION REQUESTED
11   PAGE   LINE
12   (NONE)
13
14   DOCUMENTS REQUESTED
15   PAGE   LINE
16   (NONE)
17
18   WITNESS INSTRUCTED NOT TO ANSWER
19   PAGE   LINE
20   54   16
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1   INDEX TO EXHIBITS
2
3 EXHIBIT   MARKED
4 Exhibit QX240 Opening Expert Report of   8
                  Dr. Shuo-Wei (Mike) Chen on
5   Qualcomm Source Code
                  (Not Attached)
6
   Exhibit QX241 Source Code Production Log,   125
7   Bates QCARM_7517717 - 7517738
                  (Not Attached)
8
   Exhibit QX242 Arm Architecture Reference   131
9   Manual, Armv8, for A-profile
                  architecture
10
   Exhibit QX243 ████████████████████   133
11   ██████
                  (Not Attached)
12
   Exhibit QX244 Arm 2020 Architecture   135
13   Extensions
14 Exhibit QX245 Source Code Production Log,   152
                  Bates QCARM_7607814 - 7607874
15   (Not Attached)
16 Exhibit QX246 Perl.com Beginner's   160
                  Introduction to Perl - Part 2
17   (Not Attached)
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2 (Pages 2 - 5)

Page 6

1   TUESDAY, JUNE 25, 2024, 9:12 A.M.
2   LOS ANGELES, CALIFORNIA
3
4   THE VIDEOGRAPHER: This is Jacob Florez, the
5 videographer. I represent Veritext Legal Solutions in
6 Los Angeles, California. My California notary public
7 number 2365264.
8   I am not financially interested in this action,
9 nor am I a relative or employee of any attorney or any
10 party.
11   Today's date is June 25th, 2024. The current
12 time on the monitor is 9:12 a.m. We're on record.
13   This deposition is taking place at 707 Wilshire
14 Boulevard, Number 6000, Los Angeles, California 90017.
15   This is the deposition of Dr. Shuo-Wei (Mike)
16 Chen in the matter of Arm Ltd. vs. Qualcomm, et al.; Case
17 Number 22-1146 (MN), requested on behalf of defense.
18   Would counsel please introduce themselves and
19 any colleagues for the record.
20   MR. FUNG: Nicholas Fung from Morrison &
21 Foerster here on behalf of plaintiff Arm.
22   MS. NYARADY: Catherine Nyarady, from Paul,
23 Weiss, on behalf of the defendants, and I'm joined by my
24 colleagues Jacob Braly, also from Paul, Weiss, and
25 John Poulos, from Norton Rose Fulbright.

Page 7

1   THE VIDEOGRAPHER: Thank you.
2   Will our court reporter please swear in the
3 witness.
4   SHUO-WEI MIKE CHEN, Ph.D.,
5   having been first duly sworn, testifies as follows:
6   EXAMINATION
7 BY MS. NYARADY:
8   Q   Good morning, Dr. Chen.
9   A   Good morning.
10   Q   You have -- you appear to have a couple of
11 documents in front of you that you brought with you.
12   Can you tell me what those are?
13   A   Yes, one is my opening report, and the other
14 one is the reply to the doctor in the room.
15   Q   So those are two expert reports that you
16 submitted in this action; is that correct?
17   A   That is correct.
18   Q   Are those clean copies of the report?
19   A   Yes.
20   Q   No -- no annotations or marks or highlighting?
21   A   No.
22   Q   Okay. Do they have the appendix -- the
23 appendices that went with the report?
24   A   Let me check. There's --
25   Q   It might be called exhibit --

Page 8

1   A   -- my resume.
2   Q   Yeah.
3   A   Yeah, the resume.
4   Q   Does it have the list of documents considered
5 as well?
6   A   Yes. In Exhibit B, yeah.
7   Q   And what about -- that was for the opening
8 report; right?
9   A   The opening, yeah.
10   Q   So what about the reply report?
11   A   Yep, there's also material considered.
12   Q   Okay. You can feel free to obviously refer to
13 your own documents, but I am going to mark a copy of your
14 opening expert report. It should be exactly the same
15 thing that you have in front of you.
16   MS. NYARADY: We're going to mark that as
17 Exhibit 240.
18   Do I need a prefix?
19   MR. BRALY: QX.
20   MS. NYARADY: QX.
21   I'm going to mark it as QX240.
22   (Exhibit QX240 marked.)
23 BY MS. NYARADY:
24   Q   There you go. And if you could just verify
25 that that is, in fact, the same opening expert report

Page 9

1 that you submitted in this action.
2   A   Yes.
3   Q   And if you go to Page 34, please, of
4 Exhibit 240.
5   A   Yep.
6   Q   Is that your signature that appears on that
7 page?
8   A   Yes.
9   Q   Okay. If you can turn to the front of that
10 report, and you should feel free to refer to it or not in
11 order to answer my questions. But just so you kind of
12 know where I'm at, if you look at Paragraph 2 of your
13 report, you've got a section that's called Background.
14   And you talk about some of the work that you've
15 done and your expertise.
16   Can you tell me what you're an expert in that's
17 relevant to this case?
18   A   Sure. As I mentioned in this Paragraph 2, I
19 have done significant work on the digital ASIC
20 implementations, and those ASIC information requires me
21 to get involved in this RTL coding, so RTL coding is a
22 way to describe the function of the circuit that we
23 intend to implement. And that's how we can generate the
24 actual, you know, chip design.
25   For example, you know, it's part of SoC, so I

3 (Pages 6 - 9)

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1 and you weren't asked to look into any of the corporate
2 structure of what happened to NUVIA, the company, after
3 the acquisition or anything like that?
4   A   No.
5   Q   Okay. Let's go to Paragraph 18 of your opening
6 report, please.
7   A   Yes.
8   Q   So there's a subheading there that says A --
9 it's subsection A, Summary of Opinions.
10   Do you see that?
11   A   Yes.
12   Q   And it says that you were asked to perform both
13 a quantitative and a qualitative substantive analysis of
14 the RTL code produced by Qualcomm; right?
15   A   Correct.
16   Q   On the quantitative side, it says that you were
17 asked to determine the extent to which the source code
18 developed by NUVIA prior to the Qualcomm acquisition is
19 identical to source code in Qualcomm's products.
20   Do you see that?
21   A   Yes.
22   Q   You then go on to say that based on your
23 analysis, it is your opinion that substantial RTL code
24 written by NUVIA pre-acquisition is incorporated into
25 several SoCs/cores developed by Qualcomm after the

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1 acquisition; correct?
2   A   Correct.

12   Q   Okay. Were you instructed to do that, or was
13 that your choice?
14   A   I couldn't remember the detail, but it's
15 probably both because it makes sense.
16   Q   So probably in consultation with someone, you
17 chose that?
18   A   Yeah.
19   Q   Okay. And is that an accurate summary of your
20 opinion, as you sit here today?
21   A   Yes.

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19   Q   And as you sit here today, does that remain
20 your opinion?
21   A   Yes.
22   Q   Okay. The word "derivative" does not appear
23 anywhere in your opening report; correct?
24   A   I don't recall. And I cannot search this hard
25 copy.

Page 89

1   Q   Would it surprise you if I tell you that I did,
2 and it doesn't appear in the report?
3   A   Doesn't appear? That's fine, yeah.

9   MR. FUNG: Objection. Form.

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2 BY MS. NYARADY:

3   Q   Yes.

4   A   No.

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1 BY MS. NYARADY:

2   Q   And you weren't asked to do that, were you?

3   A   I was not.

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8   Q   Would your answers be the same if I asked you

9 these questions with respect to the ▮▮▮▮▮▮▮▮

▮▮▮▮▮▮▮▮▮▮

11   MR. FUNG: Objection. Form.

12   THE WITNESS: Again, I have no -- I have not

13 studied any of the contract, the issues, those legal

14 document, so I cannot offer my opinions.

15 BY MS. NYARADY:

16   Q   So just to -- just to make sure I understand,

17 so you're not intending to offer any opinions with

18 respect to these terms or derivative or things of that

19 nature -- the legal terms as used in the ▮▮▮▮▮

▮▮▮▮▮ either; correct?

21   A   Correct.

22   Q   Okay. Now, would it surprise you to learn that

23 the term ▮▮▮▮ also does not appear in your opening

24 expert report?

25   A   The term ▮▮▮▮

Page 92

1   Q   Uh-huh, yes. And I don't mean to confuse you.

▮▮▮▮▮▮▮▮▮▮▮▮

3   A   Okay.

4   Q   And so I -- would it surprise you if I tell you

5 that I did search the report, and you don't use that

6 terminology in your opening report either?

7   A   No.

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14   Q   And no one asked you to consider that

15 issue; right?

16   A   No.

17   MS. NYARADY: Why don't we take a quick break.

18   THE WITNESS: Sure.

19   THE VIDEOGRAPHER: The time is 11:31 a.m. Off

20 record.

21   (Break held off the record.)

22   THE VIDEOGRAPHER: The time is 11:46 a.m.

23 We're back on record.

24 BY MS. NYARADY:

25   Q   Okay. Let's go back to Paragraph 18 in your

Page 93

1 opening report. And I want to start with that first

2 quantitative opinion that we were talking about.

3   A   Sure.

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12   Q   What did you mean by "substantial"?

13   A   Substantial go by the percentage that's at

14 least in the table.

15   Q   So what percentage is substantial?

16   A   If the code are two independent developed by

17 different engineers, you know, I cannot find this level

18 of the percentage -- you know, in my experience, you

19 cannot have this level of percentage of similarity.

20   So I was comparing against those scenario like

21 that. And that I conclude is a substantial.

22   Q   Where is the cutoff? At what point does it

23 become not substantial? What percent?

24   A   I don't have a particular -- I did not offer

25 any particular opinions, you know, on those. But the

24 (Pages 90 - 93)

Page 94

1 things that -- you know, you have two very different RTL
2 code, the designs. You know, you'll be probably matching
3 those unrelated, you know, codes, like, spaces, you know,
4 things like that.
5   I don't know. So that's, you know -- it's very
6 insignificant portion of the whole files.
7   Q   But there's no absolute percentage that you
8 have in mind where -- where something crosses over to
9 being substantial, is there?
10   A   No. I don't -- I don't have those.
11   Q   And that's not like an industry standard term,
12 saying "substantial," is it?
13   A   No.
14   Q   Okay. Was there any kind of test or
15 methodology that you used in -- in kind of formulating
16 what was substantial, or it's just these percentages
17 struck you as substantial?
18   MR. FUNG: Objection. Form.
19   THE WITNESS: Yes. So it's many, you know,
20 going for those percentage that I analyze, and the two
21 allow me to see the codes side by side.
22   And I can see, you know, those similarity
23 right, to the left, you know, the two sides, and that's
24 how I, you know, make this opinion.
25 ///

Page 95

1 BY MS. NYARADY:
2   Q   So would you agree with me that it's, to some
3 extent, subjective, your determination of what is
4 substantial?
5   MR. FUNG: Objection. Form.
6   THE WITNESS: Yes, in that paragraph, yes.
7 It's substantial. And that's why I also create those
8 tables to have more quantitative numbers, yes.
9 BY MS. NYARADY:
10   Q   In that section, that sentence that we're
11 looking at, you also say, "incorporated into."
12   Do you see those words? You're talking about
13 the pre-acquisition code being incorporated into
14 post-acquisition SoC/cores.
15   A   Yes.
16   Q   What do you mean by "incorporated into"?
17   A   Yes. So similar to what I mentioned earlier on
18 the similarity, on the two designs, it's clear to me that
19 they would actually inherit on the previous designs.
20   For the most obvious -- the first reason that
21 I've seen is the file name similarity. So the file names
22 are those RTL codes that create by the engineers.
23   And when I first, you know, examined the code
24 database, most of the file names are -- strike to me that
25 they are just the same; right? And you can see some of

Page 96

1 the entry. Here, for example, in Table 2, in my opening
2 report, I even see a folder where you have 100 percent
3 match. So that's what I meant by "incorporated."
4   It strike to me that, you know, this has to be
5 the code that get carried over to the next product.
6   Q   So is it accurate to say that by "incorporated
7 into," you mean a direct copy?
8   MR. FUNG: Objection. Form.
9   THE WITNESS: I shouldn't say direct copy. You
10 know, it's just the design -- you know, when you design a
11 new circuit, a new design, what's your base that you
12 design -- you started from?
13   Do you start from scratch or you start from,
14 you know, a prior design database. And that's what I
15 meant. So you would have that design database as a
16 starting point, and then you can do the further
17 modification, yeah, so that's what I meant.
18 BY MS. NYARADY:
19   Q   Your opinions are -- you're going -- starting
20 to go into some of the tables in your report.
21   Your opinions are limited -- are they not? --
22 to the 14 folder paths that you have set out in Table 1?
23   MR. FUNG: Objection. Form.
24   THE WITNESS: In the whole quantitative
25 analysis, those in Table 1, those are the -- indeed the

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1 folder that I consider for generating those quantitative
2 analysis. That is correct.
3 BY MS. NYARADY:

22 BY MS. NYARADY:
23   Q   The comparison that you ran, does it just tell
24 you whether lines of code are identical? Let's put --
25 sorry, let me -- you mentioned the file names. Let's put

25 (Pages 94 - 97)

Page 98

1 aside the file names.
2   But when we're talking about line similarity,
3 does it just tell you whether lines of the code are
4 identical?
5   A   Yes, when you put the RTL code side by side.
6 Because the RTL is a hardware description on what they
7 actually tried to implement, yes. So under that
8 constructions; right?
9   You say this line, okay. You're trying to
10 implement this particular register, for example, do you
11 also have the corresponding line of code? Okay. So also
12 want to implement that particular register. If they all
13 match, then they will match as identical lines.
14   Q   And the program that you used is not doing any
15 analysis -- is it? -- as to whether any individual line
16 relates to the Arm architecture?
17   MR. FUNG: Objection. Form.
18   THE WITNESS: The uncompared tool is a base --
19 based comparison tools. So you would look at the RTL
20 codes, and they would try to match, you know, each
21 character to each character and then to see whether they
22 would -- whether there's any difference or they're
23 identical, things of that nature.
24 BY MS. NYARADY:
25   Q   But it's not doing a substantive analysis of,

Page 99

1 again, for example, whether that line of text relates to
2 the Arm architecture?
3   A   No. It's just between the two files under
4 comparison, they would see how similar they are, either
5 identical or maybe something could change. Maybe you add
6 one more space.
7   Q   I think of it a little bit like -- because in
8 my world, we have more Word documents; right? And you
9 can run a comparison of two files and get what we often
10 call a redline of -- of the changes in a document.
11   Is it doing something similar to that?
12   A   It's probably doing more than that; right?
13 Because, you know, in this case, there were not just --
14 to document whether this particular word line changes,
15 but this one also have this line by line, so they go
16 line-by-line-based.
17   So it's just a lot more -- provide a lot more
18 information, and this oftentimes is quite useful in our
19 engineering world, especially RTL code because it's
20 really hardware description.
21   So by doing this line-based, you know, matching
22 process, it just give the engineer information on, you
23 know, what has been changed and exactly what section of
24 the code has been changed. Just easier for us to debug
25 or make changes.

Page 100

1   (Reporter clarification.)
2   A   Debug or make changes.
3   Q   When it's doing the line comparison, is it
4 grouping lines? So let me make sure I'm explaining my
5 question.
6   If you have the original file and you have
7 lines 1 through 5 of the code --
8   A   Uh-huh.
9   Q   -- is the tool looking to see whether those
10 lines 1 through 5 are identical and in the same order and
11 consecutive in the other file, or is it looking first for
12 is line 1 there somewhere? Is line 2 there? Is line 3
13 there?
14   Do you understand my question?
15   A   Yeah. I don't know the exact algorithm they
16 use under the tool. But the net outcome is that -- so
17 let's say you have 1 to 5; right -- or 1 to 1000,
18 whatever, and then the other side was 1 to 1000, so what
19 they would do is though would try to do alignment,
20 something that causes alignment.
21   So they would align that, hey, maybe -- as you
22 mentioned, maybe there's a block of the code. So let's
23 say there's five lines, 1 to 5. It matched to 21 to 25
24 for the other code. Then they would say, hey, you know
25 what? I found that they actually are the same. Then

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1 they would align this, you know, and then they can
2 further compare that, whether they're identical or maybe
3 hey, this line number two, somebody change the name of
4 that register, for example.
5   Then they would try to show up what are the
6 changes.
7   Q   Okay. And so in that instance -- right? -- if
8 it locates lines 1 through 5 and it found there was a
9 change in line 2, would the output then say four lines
10 are identical?
11   A   Yeah, so they have some reports, yeah. So they
12 would say how many are identical. How many are changed.
13 How many lines are added as new lines.
14   Q   Uh-huh.
15   A   Some may be completely deleted.
16   Q   And the algorithm -- so I mean, just -- just --
17 I guess let's be more specific about what we're talking
18 about.
19   We're talking about the Beyond Compare tool;
20 right?
21   A   Correct.
22   Q   That's what you used?
23   A   Correct, correct.
24   Q   And that is a third-party software?
25   A   Correct.

26 (Pages 98 - 101)

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1 Q And it's used to compare code in various ways?
2 A Correct.
3 Q Okay. And that's proprietary; right?
4   MR. FUNG: Objection. Form.
5 BY MS. NYARADY:
6 Q The software? I mean, you just testified a
7 second ago that you don't know the details of the
8 algorithm. And, in fact, the algorithm is proprietary to
9 the company that makes that software?
10 A Right.
11 Q So none of us know exactly what the algorithm
12 is that that tool uses to make this comparison; right?
13   MR. FUNG: Objection. Form.
14   THE WITNESS: Different algorithm has different
15 efficiency. You know, how fast they can generate a
16 report. So yeah, to that level, we don't know. But the
17 outcome is what I described.
18   You know, they would find a matching line. If
19 they have a SKU, they would do an alignment. They would
20 go line by line and check, you know, is there any
21 difference or are they identical.
22 BY MS. NYARADY:
23 Q So if in -- back to our kind of hypothetical,
24 where I was saying if you have five lines of code.
25   If only one line was identical and it was found

Page 103

1 somewhere in the file that you're doing the comparison
2 with, that would be reported as an identical line;
3 right --
4 A Yes.
5 Q -- to your knowledge?
6 A Yes. If there was only one line that match, it
7 would say only one line would match, yes. And then they
8 would -- so this line similarity is a percentage. Then I
9 would find how many identical lines, divide it by the
10 total number of lines, and that give you the percentage.
11 Q In Paragraph 18, just back to the sentence we
12 were looking at, you did use the term SoCs/cores; right?
13 A Yes.
14 Q In this context, what do you mean by "core"?
15 A Cores -- you know, remember we discussed NCC,
16 and on the NCC there are four different CPU core, so
17 that's what I meant by core.
18 Q And the cores that you analyzed are the ones --
19 the code snapshots, if you will, that are set forth in
20 your tables headings?
21 A Yes. Yes. So you see the table, there's a
22 folder path. So that's correspond to the specific source
23 code hierarchy.
24   And under the hierarchy, the white inside those
25 are the analysis that we just discussed using

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1 Beyond Compare, and we say file name, what similarity,
2 line, what's the similarity.
3 Q And for each of the products or each of the
4 working projects, if you will, you did not necessarily
5 review all of the cores, did you?
6   And let me -- let more be specific. I don't
7 want you to be guessing as to what I'm asking.
8   For some of the products, there are both large
9 and mid-sized CPU cores; right?
10 A Some of the later products, yes.
11 Q Right. So like the ███████████████
12 ███████████████████████; right?
13 A Sounds about right, yeah. But I need to
14 actually go to check exactly what product, yeah.
15 Q Fair enough. Fair enough.
16   So some of the later products --
17 A Later conversions, yes.
18 Q Right. And you did not do this analysis for
19 the midsize CPU cores; right?
20 A I did not.

Page 105

7   MR. FUNG: Objection. Form.
8
15 A And for me to do this comparison is to really
16 find the corresponding file path, to have both
17 comparison.
18 Q In terms of identifying the 14 folder paths
19 that we've talked about in Table 1, did you identify
20 those by yourself, or was it in conjunction with counsel
21 or speaking to anyone?
22 A It's mostly by myself and the NUVIA technical
23 document.
24   (Reporter clarification.)
25 A Technical document.

27 (Pages 102 - 105)

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1	Some of the document actually show the
2	hierarchy, so this is design hierarchy of the, let's say,
3	SoC or the NCC.
4	So from there, actually, it helped me a lot to
5	anchor my focus; right? They would say okay. These are
6	NCC. Remember I mentioned about this four CPU cores, so
7	it's all very clear, you know, in the technical document.
8	And what I did is look at this technical
9	document. Then I go to the source code machines, and I
10	follow this file structures and I can see the mapping.
11	So -- and that helped me a lot to actually identify, you
12	know, in this case, you know, the 14 folders; right?
13	So you have this, you know, for example, COR
14	that represent the CPU core. You have this IFU unit, for
15	example. I can also see that -- the technical document,
16	so they just have this mapping, and that actually helped
17	me to traverse, you know, through this hierarchy.
18	Q	So you may have already just answered in part
19	what was my next question. And if you want to look at
20	the report, it's in Paragraph 26.
21	You talk about your analysis of the source
22	code, and you say you identified key folders; right?
23	A	Yes.
24	Q	So the process that you just described, is that
25	how you identified key folders?

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1	A	Yes.
2	Q	And what is it about those folders that made
3	you deem them key?
4	A	Yeah, so that would be the CPU, so actually the
5	NCC because, you know, NUVIA, I think, CPU cluster.
6	So -- and then from there, there's a CPU core. And in
7	the document that provide by the NUVIA, they actually
8	identify, okay, this is CPU core. And those are the
9	subsequent function that was built as a unit as part of
10	the CPU agent.
11	So they actually have a nice table at least in
12	their document, so I just basically just follow those and
13	then traverse through.
14	Q	So is it fair to say that your -- your focus
15	was on the core; right?
16	A	In this case, yeah, because that should -- as I
17	said, you know, that's the center part of the processors.
18	So that would just help me to identify a more direct
19	evidence, you know, of the CPU architectures.
20	Q	Because I know you also note -- and this was in
21	Paragraph 25 -- but you note there was a lot of code in
22	the -- I believe it's in Paragraph 24 where you talk
23	about --
24	A	Yes.
25	Q	-- you know, the number of files and all of

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1	that.
2	And so you did not do this comparison across
3	all of those files; right? You did the comparison on
4	select files that you deem key, and my understanding is
5	that those all relate to the core?
6	MR. FUNG: Objection. Form.
7	THE WITNESS: Yes.
8	BY MS. NYARADY:
18	Q	You were trying to capture the same concept?
19	A	The same concept, yeah. The percentage is
20	high.
21	Q	And the same question that I asked you with
22	substantial. For significant, is there an
23	industry-defined number, you know, at which point it's
24	significant?
25	A	No.

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1	Q	Are there any folders or files that you've ran
2	the Beyond Compare tool on that you did not put the
3	results of in your report?
4	A	No. The qualitative are the ones that I just
5	mentioned, all of those folders. Some of the -- sorry,
6	these are quantitative.
7	On some of the qualitative analysis, some of
8	the file that I look into may be outside of the folder
9	that I mentioned here. But that's the second sections.
10	Q	Okay. But for the quantitative portion, all of
11	the results of the Beyond Compare that you ran would
12	appear in the tables in your report.
13	Is that accurate?
14	A	Correct.
15	Q	And you've said that your opinions on these
16	quantitative portions of the report are based on the
17	output that you got from the Beyond Compare tool; right?
18	A	Yes. The similarity test.
19	Q	Okay. And you said, I believe, in your report
20	or in one of your reports that you use the default
21	settings of Beyond Compare; correct?
22	A	Correct.
23	Q	So were there any settings on the tool as you
24	found it on the review platform that you changed?
25	A	No.

28 (Pages 106 - 109)

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1   Q   I know one setting was this SKU tolerance. And
2 we're going to talk about that.
3   But what other settings were in the default
4 other than the SKU tolerance?
5   A   I did not really investigate that part, so I
6 have no knowledge to comment -- to offer my opinions.
7   Q   So the SKU tolerance, you said you used the
8 default, which was 2,000 lines above or below the current
9 line; correct?
10   A   Correct.
11   Q   Did you run any comparisons with any other SKU
12 setting?
13   A   I did not do as comprehensive as what I did
14 here, meaning compare all of the folders across all of
15 the SoC versions. But there was one test that I did.
16 You probably noticed the percentage would change as the
17 time goes on; right?
18   The time goes on. The more changes that I made
19 to the -- to the codes. And then you would see that --
20 you know, you can imagine the engineer would say okay.
21 Let me insert another modules.
22   So there was one instance where I look at the
23 files. I say, hey, you know what -- because they
24 actually show you file A, file B next to each other. And
25 I look at the instance. I look and say, Hey, you know,

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1 that actually the same module. I seen that.
2   How come they did not identify it? They are
3 identical. That's how I realized that, okay, there's
4 some setting in the tool, that so-called SKU tolerance.
5 So they will not look all of -- all of the lines, you
6 know, it's not like, okay, this lines then you would
7 search the entire, let's say, 1 million lines on the
8 other files.
9   So they would only look at the portion, as you
10 just mentioned, and also in my report that threshold --
11 that SKU threshold. So that's the boundary that the
12 tool -- tool set to look for this alignment.
13   And once you align, then they will compare. So
14 that's how I found it. And then I -- I think I might
15 have changed that SKU tolerance. So, for example, you
16 know, it increased a lot. And I say okay. Now it's
17 aligned. Now it's aligned. And that's how I realized,
18 okay, there's indeed sections -- a parameter that you can
19 change.
20   And sure enough, you know, when you do this --
21 when you increase the SKU tolerance, the time it takes to
22 do the comparison also increase. And it increase
23 notably, you know, even I can tell as a human.
24   So -- and that, you know, later on, I think in
25 one of my report -- maybe reply report -- you know, I

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1 then find out the documentation from the Beyond Compare,
2 they actually mention this. As you increase this
3 tolerance, yes, the accuracy will improve for this
4 alignment. But your time will also increase.
5   Q   So the answer to my question about whether you
6 ran comparisons other than the 2,000 line SKU tolerance
7 is yes, you did?
8   A   For that one instance.
9   Q   For just one file?
10   A   One case. One case, yes.
11   Q   Okay.
12   A   For the one particular case, yes.
13   Q   Do you -- and that's not in the report
14 anywhere; right?
15   A   That's not in the report.
16   Q   Do you recall which file it was for?
17   A   I don't recall.
18   Q   Okay. Did you do that before or after you had
19 run the simulations -- I'm sorry -- the comparisons at
20 the 2,000 default?
21   A   I don't recall. I think that's probably
22 towards the end of the code review, yeah.
23   Q   Okay. And is -- you did it on one file and
24 that's it?
25   A   Yes.

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1   Q   Okay. Had you used the Beyond Compare software
2 prior to using it in this case?
3   A   I don't recall from my recollection. But for
4 sure, I used similar tool. There are different
5 third-party tools that can do this --
6   (Reporter clarification.)
7   A   Third-party tools.
8   Q   There are, as you said, different third-party
9 tools that do similar comparisons.
10   Are you familiar with the one called Patience
11 Diff algorithm?
12   A   No.
13   Q   Have you heard of the Myers and Bram Cohen
14 algorithm?
15   A   No.
16   Q   Are there any algorithms that come to mind that
17 you know that you have used prior to today to do such a
18 comparison?
19   A   Yeah, I don't -- I don't recall. The only
20 thing I remember about the tool that I used, are always
21 Linux -- Linux framework.
22   Q   And there are tools -- right? -- where the
23 algorithm is not proprietary other than Beyond Compare?
24   MR. FUNG: Objection. Form.
25   THE WITNESS: I'm not sure. I did not study

29 (Pages 110 - 113)

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1 that aspect.
2 BY MS. NYARADY:
3   Q   Okay. So with any of your work at USC, do you
4 use Beyond Compare?
5   A   Not particularly. But I think some of my
6 student actually use Beyond Compare.
7   Q   But you don't?
8   A   I don't particularly remember.
9   Q   Now, there is a -- based on your prior answer,
10 maybe you're not sure.
11   But are you aware that there is a setting
12 regarding important and unimportant lines in the default
13 settings on Beyond Compare?
14   A   No. Everything I use default.
15   Q   Okay. Do you know how the default determines
16 whether a line is important or unimportant?
17   A   I had some experiment because I look at the
18 report that would say it's unimportant lines. And then
19 I -- because they actually have some color. They would
20 show up as color. They show up color different if that's
21 important or unimportant.
22   The one that I have noticed, the one by
23 default, if that's unimportant, basically you just
24 white-space line. So -- so that one I know that
25 Beyond Compare would consider if you just hitting the

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1 enter, you have a bunch of white space and then they
2 would say it's unimportant lines.
3   Likewise, in one of my, I think, reply report,
4 I also did experiment. So let's say you have two
5 identical lines and that just add one space -- just one
6 space, then they will flag, okay, that's different.
7 That's different.
8   But then they would say it's unimportant.
9 Because I think what that means is that because you just
10 add one space, even though they are different, it's
11 unimportant. So that's to the extent that I understand
12 regarding this.
13   Q   Beyond Compare would deem code comments as
14 important; correct?
15   MR. FUNG: Objection. Form.
16   THE WITNESS: I did not specifically check
17 that, but I expect that it's possible.
18 BY MS. NYARADY:
19   Q   And the comments in -- you know, when I use the
20 term "code comments," that's non-functional text --
21 right? -- that appears in the code?
22   A   Correct. Usually the comment is for engineers
23 to remind themself, what's this line of codes, what --
24 what you're trying to do as a reminder, as a note.
25 That's the common practice.

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1   Q   And sometimes you put it in, so that if someone
2 else is looking at your code, too, it helps them follow
3 it?
4   A   Correct, yeah, for documentation in a way.
5   Q   And Beyond Compare also would -- are you aware
6 that Beyond Compare would also deem headings as important
7 lines?
8   A   I did not specifically check that, but it's
9 possible.
10   Q   Okay. It wouldn't surprise you if that were
11 true?
12   A   It wouldn't surprise me.
13   Q   Okay. And headings, similarly, are
14 non-functional code; correct?
15   MR. FUNG: Objection. Form.
16   THE WITNESS: What type of heading that you're
17 referring to?
18 BY MS. NYARADY:
19   Q   Well, what is a heading in -- in RTL?
20   A   So basically you may have some heading to
21 incorporate some of the libraries, you know, functional
22 blocks that you want to include that can be part of the
23 headings.
24   So basically it's a setup for the RTL code.
25   Q   Would it actually call to some -- some other

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1 software, the heading that you're talking about?
2   A   It can call another RTL code. Basically it is
3 the design where we call it a hierarchy design code
4 because oftentimes in order to have the manageable design
5 database, it's better that, you know, you would divide
6 RTL into different files.
7   So you have different functions, different
8 modules, and then you can incorporate that, you know, for
9 this particular RTL code that you're trying to do.
10   Q   Does the term "heading" mean anything else in
11 the context of -- of RTL?
12   A   That's my understanding as I described as the
13 heading of the RTL code.
14   Q   So I just want to make sure I'm understanding.
15   Is it your testimony that a heading is always
16 functional?
17   A   That's one example of the headings.
18   Q   Okay. So are there other examples --
19   A   There could be some other headings, yes.
20   Q   And sometimes they can be
21 non-functional; right?
22   A   Yes, sometimes it can be for simulation
23 purpose, for example, I want to set up time scale. You
24 know, when someone take this RTL code for the simulation
25 purpose, then they will give you some guidance of what

30 (Pages 114 - 117)

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1 it's citing.
2   Q   And you don't know one way or the other, do
3 you, whether Beyond Compare, when it's set to the default
4 settings, would capture as important lines non-functional
5 headings, do you?
6   A   Beyond Compare tool, I don't think that it can
7 differentiate what is a functional code or non-functional
8 code. It's completely text-based comparison tools, yes.
9   So you would just look at this line of code and
10 that line of code and whether that's identical or not.
11   Q   And it would include that as important
12 lines; right?
13   A   It's possible, yes.
14   Q   It wouldn't surprise you if that were the
15 case; right?
16   A   Yes.
17   Q   Okay. What about with respect to, for example,
18 copyright notices that are in the code? Do you know
19 whether Beyond Compare would deem that important or
20 unimportant lines?
21   A   It -- again, it wouldn't surprise me if they
22 would flag that as important lines, yes. But I have to
23 say that most of the RTL code that I found, most of the
24 lines are the body of the actual RTL description, you
25 know, the comments, headings. Usually it's just small

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1 portion of the whole file.
2   Q   And the copyright notices similarly are
3 non-functional text; right?
4   A   Yeah, like comments as an example.
5   (Reporter clarification.)
6   A   Like comments as an example.
7   Q   Did you look at the code that was found to be,
8 for lack of a better term, you know, uncommon between the
9 two snapshots that you were comparing?
10   Did you actually look at the code to determine
11 the substantive or functional nature of the code?
12   MR. FUNG: Objection. Form.
13   THE WITNESS: Yeah, so initially when I run
14 this test, you know, I need to first make sure it's doing
15 the right thing; right?
16   So let's say -- let's -- for example, you know,
17 if I take the top-level NCC, right, the cluster, RTL
18 files, and I would see side by side, and I would, see
19 okay, yeah, so this one is the four CPU core, and that
20 one was four CPU core, and they match; right.
21   So this is more like manual checking just to
22 confirm that, yes, the Beyond Compare tool, you know,
23 come from these two RTL code are identical, and I can
24 interpret, you know, the designers, right, as human
25 engineers to say that, yes, its extension is core. Okay.

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1 Yes, that one also extension is core. So that extent,
2 you know, I do this kind of check.
3   Again, the Beyond Compare tool is not the RTL
4 simulation tools. So it cannot show the result or the
5 function of that particular RTL code.
6 BY MS. NYARADY:
7   Q   So if I understand your testimony, I mean, you
8 did -- you did a good check. So when you started using
9 the tool, you kind of eyeballed it to make sure that you
10 thought it was doing the comparison that you understood
11 it to be doing; right?
12   A   Correct.
13   Q   But you didn't -- once you satisfied yourself
14 of that, for each of the comparisons that you did, you
15 didn't check all of the code as it was compared in each
16 of the files, did you?
17   A   So all of the files here, I did not check every
18 single one of them. However, as you can see, in part of
19 any quantitative analysis, there is some file I
20 particularly single out, which --
21   Q   Right. I guess -- and that's a fair comment.
22 I've been meaning to ask you questions about the
23 quantitative portion.
24   A   Okay. Sure.
25   Q   So you're absolutely correct. I understand

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1 there are some specific examples in the qualitative
2 portion of your report.
3   Other than those and kind of this gut check
4 that you did in the beginning, did you look more
5 specifically, you know, at the code in the individual
6 files or folders to see what type of code it was, whether
7 it was functional, what it was doing, whether it involved
8 the Arm architecture, you know, those kinds of things?
9   Did you do that analysis?
10   A   Yeah, so that would be in the qualitative
11 report. So if I go to look for specific line of codes to
12 whether that's complying to specific CPU architecture, as
13 an example, that I put in the qualitative analysis.
14   But for the quantitative analysis, I said, you
15 know, once I confirmed -- so let's say, this individual
16 file, it looks -- making sense to me, then I just let the
17 tool to run the entire statistical comparison.
18   Q   Now, you also -- I've been asking you a lot of
19 questions about the line comparison; right?
20   A   Uh-huh.
21   Q   You also did, as you mentioned earlier and is
22 in your report, you did a file name similarity
23 comparison; right?
24   A   Correct.
25   Q   Is file name kind of exactly what it sounds

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1 like? Is it -- is it the name that a certain module or a
2 certain file is given in the -- in the snapshot?
3   A   Yeah, so the file name in this case is RTL file
4 name; right? So remember that example I show you on this
5 different RTL file, NCC_NCC.SV, so that is what I define
6 as a file name of that particular RTL code; right?
7   So I just look at, for example, in this case,
8 let's say NCC_NCC.SV, so let's say that happens in Orion
9 folder and if I go to the next one, so let's say, I go to
10 Pegasus, right, or Hamoa and I go to the same folder. If
11 I see NCC_NCC.SV, so they're identical. Then this -- the
12 tool will flag as identical file name. That's what I
13 meant.
14   Q   The file name in and of itself is
15 non-functional; correct?
16   A   Correct. That's the choice of the designers.
17   Q   And just for my own clarification, would you
18 ever call a file name a heading?
19   Are those -- in your terminology, those are
20 different things?
21   A   I wouldn't call that as the headings. I would
22 just call that file name or RTL.
23   Q   Okay.
24   A   Yeah.
25   Q   Now, you mentioned that when it's doing the

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1 line comparison, one example you saw was that if there
2 was extra spacing, that would be -- the lines could be
3 essentially deemed the same even though, you know, one
4 had a space and one didn't.
5   Did I understand that right?
6   A   I think it should be the opposite. So let's
7 say, you have this line of code. They are the same. But
8 if you adjust one spacing, they will flag as a different.
9   They will --
10   Q   Okay. So any change -- so let me ask you this:
11 When you talk about line similarity, does that mean it's
12 exactly the same in one database than the other?
13   A   Yes. It has to be exactly the same to be
14 qualified as identical lines.
15   Q   Okay.
16   A   Not even with one space that you insert.
17   Q   And what are orphan files?
18   A   Orphan files just means that you don't find the
19 corresponding file, so it's orphan. So it creates -- so
20 maybe engineer create new line of code which does not
21 exist in the other file.
22   Q   How does the tool deal with orphan files?
23   A   I believe they will report it. So they will
24 report -- so when they gave you the so-called statistical
25 report, you know, they will tell you how many identical

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1 lines and how many lines are changed, deleted or how many
2 are orphaned, yeah.
3   Q   And would the orphan file count have rolled up
4 into your percentages?
5   A   I don't recall specifically what's the
6 percentage of the orphan lines. But orphan line is
7 considered a different line. If I create something
8 that's different, it's not a match; right?
9   So it wouldn't count it as part of this line
10 similarity. The line similarity has to be something that
11 the tool identify they are identical.
12   Q   Right. Would the orphan files, though, be
13 accounted for in the denominator when you're coming up
14 with a percentage of line similarity?
15   A   Yes. If that's in that original file, the
16 source file, yes. So you have -- because that counts as
17 a total line, yes, correct. So your percentage would --
18 would drop if you have a lot of orphan line, percentage
19 in line similarity.
20   Q   In your report, you use the term a couple of
21 times "naming convention," and you say that the naming
22 convention was -- you know, I believe the term you use is
23 inherited across the various code bases.
24   I just want to make sure I understand what you
25 mean by that.

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1   Are you simply referring to file names when you
2 talk about naming convention?
3   A   Yes. The file name of those RTL codes, yes.
4   Q   And it's possible -- right? -- that you could
5 have the same naming convention or have the same file
6 name across two code bases but all of the RTL in those
7 files could be different; right?
8   A   Correct.
9   MS. NYARADY: I'm going to hand you what has
10 been marked as QX241. And this is a document
11 Bates-numbered QCARM_7517717 through 737 -- oh, no --
12 738.
13   (Exhibit QX241 marked.)
14 BY MS. NYARADY:
15   Q   Is QC -- sorry, QX241, is that an example of a
16 printout of one of these Beyond Compare comparisons that
17 we've been talking about?
18   MR. FUNG: Objection. Form.
19   THE WITNESS: Yes, so in the first few pages,
20 whenever you see a table-like pages, those are the Beyond
21 Compare reports.
22 BY MS. NYARADY:
23   Q   So is it just the first few pages that are from
24 Beyond Compare, or is this entire document --
25   A   Oh --

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1   Q   -- in Beyond Compare output?
2   A   Yes. So the one that you see like a template,
3 that's the whole folder comparison; right? The pages
4 that has, you know, like how many orphan lines, different
5 lines, those are the file comparison; right?
6   Because remember, I have two type of
7 comparison. One is the entire folder. The other one is
8 just individual RTL file, yes. But they are all
9 Beyond Compare report.
10   Q   And so it is output of the type in QX241. And
11 we've got, you know, several others that were produced as
12 a result of the comparisons that you did.
13   And I'm going to attempt not to mark all of
14 them, but it is this type of a report -- right? -- that
15 forms the basis for the tables that we see in your
16 opening expert report on the quantitative portion; right?
17   A   Correct.
18   Q   Was there any other data or basis for the
19 tables in your quantitative portion of the report other
20 than the Beyond Compare output?
21   A   No.
22   MR. FUNG: Objection. Form.
23   MS. NYARADY: What's the form objection?
24   MR. FUNG: It's vague and misleading.
25   MS. NYARADY: In what way?

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1   MR. FUNG: He's already testified that beyond
2 doing -- you want me to explain this?
3   MS. NYARADY: Yeah.
4   MR. FUNG: Okay. He's already testified that
5 beyond running the Beyond Compare, he double-checked his
6 work. And he ran -- he looked at the files and made sure
7 that the Beyond Compare was functioning as he thought it
8 would.
9   So that's why I objected to your question as
10 vague.
11   MS. NYARADY: So because you want him to say
12 extra in the answer, that makes it vague and misleading?
13   MR. FUNG: Yes.
14   MS. NYARADY: I don't think the question was,
15 you know -- maybe he didn't give the answer you wanted,
16 but okay. I'll let it stand.
17 BY MS. NYARADY:
18   Q   The Beyond Compare tool, when it does its
19 comparison, it's not accounting in any way for the origin
20 of the code, is it?
21   A   Can you please clarify what is origin of the
22 code?
23   Q   Does it care whether it came from NUVIA or
24 Qualcomm, for example?
25   A   No. So it's two files --

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1   Q   It's just comparing two files?
2   A   Yes.
3   Q   It doesn't care where they came from?
4   A   Correct.
5   Q   It's not analyzing where it came from?
6   A   Correct.
7   Q   It's not analyzing the date of creation?
8   A   No. It's creating the outcome, which is RTL
9 files, and of course this RTL file come from different
10 SoC core generations, yes.
11   Q   Presumably; otherwise, you wouldn't have to
12 compare?
13   A   Exactly.
14   Q   Okay. But it's not -- it doesn't know the date
15 of creation, who created it, and it's agnostic to
16 that; right?
17   A   Correct.
18   Q   Okay. So in your -- continuing with your
19 quantitative opinion, there's a point at which you
20 create -- you compared two versions of ██; correct?
21   A   Correct.
22   Q   It looks like we're on Table 12. No. Yes.
23   Well, we start with Table 12, and then we have
24 Table 13; right?
25   A   Correct.

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1   Q   Okay. Why were you comparing two different
2 versions of Orion?
3   A   Yeah, I was asked to do this analysis because I
4 think there was -- I don't recall exactly what's the
5 event. But I wouldn't be surprised if that has something
6 to do with the termination of the home license or the
7 swap-out process, either one of those.
8   Unfortunately, I don't recall the exact event.
9   Q   Other than running a comparison of two
10 snapshots of the ██ code, were you asked to do any
11 other analysis regarding the swap-out?
12   A   I did not.
13   Q   Okay. Do you have an understanding of what the
14 swap-out entailed?
15   A   I did not.
16   Q   Okay. That's just not something you were asked
17 to opine on?
18   A   No.
19   Q   And you didn't do any kind of an analysis about
20 whether any code was downloaded or retrieved from Arm
21 under either the NUVIA contract or the Qualcomm contract,
22 did you?
23   A   No.
24   Q   You weren't asked to do that?
25   A   No.

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1   Q   And the Beyond Compare tool would not assess
2 that in any way; right?
3   A   No.
4   MS. NYARADY: You guys want to take a lunch
5 break?
6   MR. FUNG: Sure.
7   THE VIDEOGRAPHER: Off record. The time is
8 12:46 p.m.
9   (A lunch recess was taken.)
10   THE VIDEOGRAPHER: The time is 1:42 p.m. We're
11 back on record.
12 BY MS. NYARADY:
13   Q   Okay. I want to talk a little bit now --
14 switch gears and talk about the qualitative opinion in
15 your opening expert report.
16   A   Okay.
17   Q   Your qualitative opinion relates to opcodes,
18 registered definitions, and then the architecture
19 extensions; correct?
20   A   Correct.
21   Q   Okay. Let's go to Paragraph 37, please, of
22 your report.
23   A   Sure.
24   Q   And here we've got under the heading of the
25 summary of the qualitative approach, you say that you

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1 reviewed -- "First, counsel for Arm identified for me the
2 Arm Architecture Reference Manual v8.7 (G.b)."
3   Then there's the Bates number ARM_01324149.
4   And then there's another parenthesis that says
5 Arm ARM; right?
6   A   Correct.
7   Q   And that's the Arm ARM we talked about at the
8 beginning of the deposition, the Arm architecture
9 reference manual; right?
10   A   Correct.
11   Q   And so this is the version that you reviewed in
12 doing your analysis for the qualitative approach; right?
13   A   Correct.
14   Q   And when you say "counsel for Arm identified
15 for me," is that someone from Morrison & Foerster?
16   A   Correct.
17   Q   Who is it that gave you the Arm ARM? Who from
18 Morrison & Foerster?
19   A   Right. Fahd.
20   Q   Patel?
21   A   Patel, yes.
22   MS. NYARADY: Okay. So I am going to mark for
23 you and hand you QX242. It is just the first several
24 pages of that Arm ARM.
25   (Exhibit QX242 marked.)

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1 BY MS. NYARADY:
2   Q   We do have the entire reference manual
3 downloaded on our laptop.
4   A   Uh-huh.
5   Q   If you need to look at it for any reason, let
6 us know. Happy to let you use the laptop and look at it,
7 but it's -- as you know, it's a very voluminous document,
8 so we just printed the cover page and the kind of table
9 of contents.
10   But just for the record, QX242, do you see that
11 the first page there at the bottom, there is the Bates
12 number that says ARM_01324149?
13   A   Yes.
14   Q   And that is the same Bates number -- right? --
15 that you reference in Paragraph 37?
16   A   Correct.
17   Q   And do you see in the small text near the
18 copyright mark on the first page at the bottom, there's a
19 reference to capital G, period, lowercase B.
20   And that is the same G.b of the version 8.7
21 that you reference in Paragraph 37; right?
22   A   Yes.
23   Q   Okay. So this is the -- these are the first
24 ten pages of the Arm ARM that you used in forming your
25 opinions; right?

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1   A   Yes.
2   Q   Did you look at any other version of the Arm
3 ARM? I mean, you understand that there are different
4 versions of this. There's now like a v9.
5   Did you look at any other Arm ARM manuals?
6   A   No. When I was forming these opinions in the
7 report, this is the Arm ARM version that I was referring
8 to.
9   Q   Okay. So you didn't compare this one to any
10 other versions or download any other versions?
11   A   No, not that I can recall.
12   Q   Okay.
13   A   Yeah.
14   MS. NYARADY: All right. I'm going to hand you
15 what we've marked as QX243. And this is a document
16 called the ████████████████████████. It's
17 Bates-numbered QCARM_2540979 through it looks like
18 2541343.
19   (Exhibit QX243 marked.)
20 BY MS. NYARADY:
21   Q   I'll give you that one.
██ ████████████████████████████████████
██ ███████████████████████████████████████
██ ███████████████████████████████████████
██ ██████████████████████████████████████

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Page 134

[redacted]

Page 135

[redacted]

6   Q   Was this document, QX243, was that also
7 provided to you by counsel?
8   A   Correct.
9   Q   And was it also Mr. Patel who provided it to
10 you?
11   A   Yes.
12   Q   Okay. Within this manual, were you -- did you
13 just review it yourself, or were you directed by anyone
14 to any specific portion of the manual?
15   A   I reviewed it myself.
16   MS. NYARADY: I've got one more. All right.
17 I'm going to show you what we're marking as QX244.
18   There's one for you. Sorry. This is one for
19 you.
20   (Exhibit QX244 marked.)
21 BY MS. NYARADY:
22   Q   Okay. So I've handed you what we've marked as
23 QX244. It is the number -- the Bates number the furthest
24 down is ARM_00099622 through 9657.
25   And this document, at the top, it says Arm on

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1 the front, and then it says 2020 Architecture Extensions.
2   Did I read that accurately?
3   A   Yes.
4   Q   Okay. And if you look at your Paragraph 37,
5 you in the first sentence after referencing the Arm ARM,
6 you also say that counsel for Arm had identified for you
7 the Arm 2020 Architecture Extensions.
8   And then it says, paren, ARM_00099622.
9   Do you see that?
10   A   Yes.
11   Q   Okay. So the document that I've marked as
12 QX244, is that the Arm 2020 Architecture Extensions
13 document that you relied on in forming your qualitative
14 opinions that are set forth in your opening expert
15 report?
16   A   Yes.
17   Q   Okay. And this document is dated -- at the top
18 there, it says the 30th of January 2020; correct?
19   A   Correct.
20   Q   Now, there's a box on the front page.
21   Do you see where -- the title of it, it says
22 Alpha Release?
23   A   Yes.
24   Q   And then it says, "A release of an architecture
25 specification at Alpha quality status has a particular

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1 meaning," and then it goes on and there's some other
2 language there.
3   Do you have any information as to the
4 significance or lack thereof of an alpha release by Arm?
5   A   No.
6   Q   Was anything that you considered important at
7 all in forming your opinions?
8   A   I did not use that to -- as part of my
9 opinion-forming process.
10   Q   Okay. If you turn to -- it's Page 5 of the
11 manual or the document, but the Bates number at the
12 bottom ends in 626.
13   Are you there?
14   A   Yes.
15   Q   Do you see there's a Section 1.3 that says
16 References?
17   A   Yes.
18   Q   And you see the document -- it says underneath
19 that, sorry, the -- "This document refers to the
20 following documents." And then one of the documents
21 under ref number one is the Arm ARM; correct?
22   A   Yes.
23   Q   So you understand this document -- these
24 architecture specifications to be something separate from
25 the Arm ARM; correct?

35 (Pages 134 - 137)

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```
 1        MR. FUNG:  Objection.  Form.
 2        THE WITNESS:  Yeah, I'm not sure what you mean
 3  by separate from Arm ARM.
 4  BY MS. NYARADY:
 5    Q    Well, it's a different document; right?  It's
 6  not -- it's not in the Arm ARM that you reviewed; right?
 7    A    This particular document?
 8    Q    Yes.
 9    A    This cite?  Yeah, I'm not -- because you see
10  there's the document numbers, I'm not sure exactly
11  whether that matched to the version that we just talked
12  about.
13    Q    I see.  So you're not sure if that matches to
14  the version of the Arm ARM that you used in your
15  analysis?
16    A    Correct.
17    Q    Okay.  Do you understand what -- well, let me
18  ask you this:  What do you understand this -- these
19  architecture extensions to be in this alpha release?
20    A    So I focused on the portions that I cite in my
21  opening report.  And that would be -- let me check --
22  that would be on Section 4, you know, on the 54 bits of
23  IPA and PA space.
24    Q    But what -- what is this document?
25    A    That's the extensions that I'm providing that
```

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```
 1  allow the users, the designers to adopt such features.
 2    Q    And are these in the Arm ARM?
 3    A    I did not particularly check whether that was
 4  in any particular Arm ARM at that time, but...
 5    Q    Okay.
 6    A    Yeah, but my understanding, you know, would be
 7  that would be additional document that talk about, you
 8  know, features or retention that we try to release beyond
 9  what they had at the time.
10    Q    So I'm just -- I'm just trying to kind of
11  establish in terms of process.
12         You looked at the Arm ARM, and then you also
13  looked at this document.  Let me see if I can help.
14         Do you understand that the 2020 architecture
15  extensions in alpha release were not yet incorporated
16  into the then-current Arm ARM?
17    A    Yes.
18    Q    And at some point later --
19    A    Yes.
20    Q    -- they may have been?
21    A    They may have, yes, yes.
22    Q    I see.  Okay.
23    A    Yes.
24    Q    And that's why you looked at this document in
25  addition to the Arm ARM?
```

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```
 1    A    Yes.
 2    Q    Because this is additional architecture
 3  specification features?
 4    A    Yes.
 5    Q    I see.  So going back to Paragraph 37, so
 6  Exhibits QX242, 243, and 244 and understanding, of
 7  course, that the Arm ARM, it's an excerpt of the full
 8  document, but those exhibits are the documents that you
 9  cite to in Paragraph 37 as forming the basis of your
10  qualitative analysis in your opening expert
11  report; correct?
12    A    Correct.
13    Q    So Paragraph 37 says that you reviewed the
14  [REDACTED]                        to identify
15  features/instructions that appear to be specific to
16  Arm; right?
17    A    Correct.
18    Q    How did you do that?
19    A    I would -- so they have sections.  So basically
20  this is a huge document.
21         (Reporter clarification.)
22    A    A huge document.
23         So what I do is that I look at the
24  instructions -- right? -- from the source code.  I can
25  identify where the instruction lies.
```

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```
 1         And I find the particular instructions, and
 2  then I would just search for this document.  And then it
 3  will identify the keyword and that would allow me to go
 4  ahead and see, you know, how that instruction was
 5  implemented.
 6    Q    I see.
 7         So you started with the code, and from there
 8  were able to identify things you wanted to search for in
 9  the -- what is exhibit QX243?
10    A    Yeah.  The exact sequence, I remember there was
11  a back-and-forth because that was initial discovery
12  process.  So I would go for this and go for that and just
13  ping pong between the two documents that helped me to
14  identify.
15    Q    Okay.
16    A    Yes.
17    Q    Did you have conversations or get any
18  assistance from anyone in this identification process?
19    A    No.
20    Q    In Paragraph 37, you go on to say that you used
21  a command line utility called grep to search for and
22  identify those specific features/instructions in the
23  March 14th, 2021, [REDACTED]  code as a baseline.
24         Do you see that?
25    A    Yes.
```

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```
 1      (Reporter clarification.)
 2   A    JSON, J-S-O-N.
 3   Q    So what is the role of the -- because I'm just
 4 not sure I completely am following -- the C and C++ files
 5 that you found, what is their role in this generation?
 6   A    Okay.  So let me give you a little bit context.
 7 You can see from Paragraph 43, you know, as I mentioned,
 8 there's some files that I found is kind of abnormal.  The
 9 files were basically missing content, you know, a bunch
10 of files that show up in Paragraph 43.
11      Then that would prevent me from checking those
12 feature ID register and the field names across different
13 SoC versions.  And because I hit that wall, I have to do
14 more search through other folders; right?
15      And hence, you know, I found that particular
16 folders, you know, the regdef and JSON file that also
17 contain that feature ID register.
18      And that's why I mentioned -- as I mentioned,
19 in order for me to have complete analysis across all of
20 the different SoC and core versions, I would turn that to
21 that JSON file.  That was the reason behind it.
22   Q    I see.  Okay.
23   A    Yes.
24   Q    And so the file that you referred to that's
25 generating the register definition files -- I'm in
```

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```
 1 Paragraph 44.
 2   A    Yes.
 3   Q    You say it's the nureg_root.cpp file that
 4 appears to generate the registered definition
 5 files; correct?
 6   A    Yes.
 7   Q    Okay.  And if the source data for that file
 8 were to change, then the registered definition files
 9 would change; correct?
10   A    Counsel, I forgot the details of that
11 particular CPP files.  I forgot, you know, what's the
12 input, what's the output, you know.  Yeah, so at this
13 point I cannot -- recall at this point.
14   Q    Okay.
15   A    Yeah.
16   Q    As a practical matter, though, I understand you
17 don't recall exactly how this happens.
18      But if you change the nureg_root.cpp file, if
19 that file is then used to generate the new registration
20 files, wouldn't the output files or the registered
21 definition file change?
22      MR. FUNG:  Objection.  Form.
23      THE WITNESS:  That really depends on that
24 files, the CPP file.  Sometimes, you know, the file can
25 be construct in a way that you would read outside
```

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```
 1 database, and you pop and generate the files.
 2      And sometimes the file can be coded inside
 3 this -- the route C file.  So there will be -- you know,
 4 you don't even need to change anything for the database
 5 coming to the CPP file.  It can be just hardware inside
 6 the CPP, and you would generate --
 7 BY MS. NYARADY:
 8   Q    I understand.  But if -- if the CPP file
 9 changed, then the file being generated from that would
10 also change; right?
11      MR. FUNG:  Objection.  Form.
12      THE WITNESS:  That depends on what you actually
13 change; right?  So if you are not changing the line
14 associated with generating this RegSet file, for example,
15 then it wouldn't change the outcome.
16 BY MS. NYARADY:
17   Q    Okay.  But if -- if the -- assuming that the
18 output depends on -- on the input that's changed, then of
19 course the output would also change; right?
20      MR. FUNG:  Objection.  Form.
21      THE WITNESS:  Yeah, I did not -- as I said, I
22 did not recall how this was instructed -- you know,
23 constructed, whether it has the input, you know, format
24 to read the database reading or generate.
25      If in a hypothetical case we say, okay, it does
```

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```
 1 read particular database file, then you would just print
 2 based on that.  Then if that changed, then the outcome
 3 would change.
 4 BY MS. NYARADY:
 5   Q    In Paragraph 46, you mentioned something called
 6 an AES field.
 7      Do you see that?
 8   A    Yes.
 9   Q    What is an AES field?
10   A    I forgot the detail of this AES field.  I think
11 it has something to do with encryption -- some encryption
12 options.  But, again, if you want to know detail, you can
13 always refer to Arm ARM documentations.
14   Q    Does AES stand for Advanced Encryption
15 Standard?
16   A    It sounds familiar, but you do need to go to
17 the Arm ARM.
18   Q    For the Qualcomm cores, who would design the
19 software driver that would utilize the AES?
20      MR. FUNG:  Objection.  Form.
21      THE WITNESS:  I did not do that part of
22 analysis.
23 BY MS. NYARADY:
24   Q    As a practical matter, would it be the partner
25 who would do that, or would it be Arm who would do that?
```

46 (Pages 178 - 181)

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1   MR. FUNG: Objection. Form.
2   MS. NYARADY: Or you don't know?
3   THE WITNESS: I cannot -- I cannot comment on
4 that. That require further analysis and standards.
5 BY MS. NYARADY:
6   Q   Do you know with respect to the underlying
7 hardware, who would design that?
8   A   Again, I did not do this part of analysis, so I
9 cannot offer my opinion.
10   Q   Okay. You don't have any information one way
11 or the other?
12   A   No.
13   Q   In Section 4, then, you're talking about the
14 architecture extension. We saw that this was the
15 architecture specification -- the alpha release document
16 that we looked at in QX244; right?
17   A   Correct.
18   Q   And you say in Paragraph 49 that you observed a
19 newly added bit; correct?
20   A   Correct.
21   Q   And a bit, again, we talked about already.
22 This is a piece of functional code; is that right?
23   A   Yes.
24   Q   And the bit itself doesn't contain any
25 information regarding a specific feature; right? I think

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1 you said you'd have to go to the documents for that?
2   MR. FUNG: Objection. Form.
3   THE WITNESS: So that's described by the
4 descriptions on later part of the Paragraph 49. You see
5 this is from the documentation; right?
6   So there was a -- if you want to do this
7 features, then you have add to this new bit. So you
8 actually do need to follow this format exactly.
9   And you see there's a bit 59. So this bit 59
10 means that position 59, so you have a string of the zero
11 and one, so that's 59 of that bit string. So it's very
12 particular.
13 BY MS. NYARADY:
14   Q   And then in Paragraph 50, you say that you
15 found a comment in the code that matches with the
16 description of the extension; right?
17   A   Correct.
18   Q   Okay. And we talked already about comments in
19 the code.
20   They're non-functional; right?
21   A   It's non-functional, but it's engineer's
22 annotation.
23   Q   Okay. And the CPU doesn't make use of the
24 comments -- right? -- in any way when it's running?
25   I mean, it's just there for the engineer's

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1 information?
2   A   Engineer information, and as we discussed maybe
3 this morning is that, you know, when you convey this code
4 to another engineers, they will read it and understand,
5 okay, this section is related to that.
6   Q   Okay. I know we talked a little bit already
7 about the opinions contained in our opening and your
8 reply report.
9   Do those reflect -- do those two reports
10 reflect the full scope of the opinions that you expect to
11 testify about at trial?
12   A   Yes.
13   MS. NYARADY: All right. Why don't we take a
14 quick break.
15   THE VIDEOGRAPHER: The time is 3:42 p.m. Off
16 record.
17   (Break held off the record.)
18   THE VIDEOGRAPHER: The time is 4:04 p.m. We're
19 back on record.
20   MS. NYARADY: We have no further questions.
21 Thank you.
22   THE WITNESS: Sure.
23   MR. FUNG: We also have no questions -- further
24 questions.
25   We reserve the right to have the witness review

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1 and correct the transcript.
2   MS. NYARADY: Before we go off the record, we
3 do have to mark the transcript as, I guess -- what is
4 it? -- highly confidential source code under the
5 protective order. Whatever the highest level of
6 confidentiality is. I think that's the right one.
7   THE VIDEOGRAPHER: Okay. The time is 4:05 p.m.
8 Off record.
9   (At 4:05 p.m., the deposition of
10   DR. SHUO-WEI (MIKE) CHEN was
11   adjourned.)
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Page 186
1   DECLARATION UNDER PENALTY OF PERJURY
2
3   I, DR. SHUO-WEI (MIKE) CHEN, do hereby certify
4   under penalty of perjury that I have reviewed the
5   foregoing transcript of my deposition taken on
6   June 25, 2024; that I have made such corrections as
7   appear noted herein in ink; that my testimony as
8   contained herein, as corrected, is true and correct.
9
10   DATED this _____ day of _____,
11 20____, at _____, California.
12
13
14
15
16
17   _____
18   DR. SHUO-WEI (MIKE) CHEN
19
20
21
22
23
24
25

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1   ACKNOWLEDGMENT OF DEPONENT
2   I, DR. SHUO-WEI (MIKE) CHEN, do hereby certify
3   that I have read the foregoing transcript of my
4   testimony, and further certify that it is a true
5   and accurate record of my testimony (with the
6   exception of the corrections listed below):
7   Page   Line   Correction
8   ____|_____|_____|_____
9   ____|_____|_____|_____
10 ____|_____|_____|_____
11 ____|_____|_____|_____
12 ____|_____|_____|_____
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17 ____|_____|_____|_____
18 ____|_____|_____|_____
19 ____|_____|_____|_____
20 ____|_____|_____|_____
21
22 Signed under the pains and penalties of perjury
23 this _____ day of _____, 20___.
24
            _____
25

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1   REPORTER'S CERTIFICATION
2
3   I, Desiree Cooks, Certified Shorthand Reporter in
4   and for the State of California, do hereby certify:
5
6   That the foregoing witness was by me duly sworn;
7   that the deposition was then taken before me at the time
8   and place herein set forth; that the testimony and
9   proceedings were reported stenographically by me and
10 later transcribed into typewriting under my direction;
11 that the foregoing is a true record of the testimony and
12 proceedings taken at that time.
13   Further, that if the foregoing pertains to the
14 original transcript of a deposition in a federal case,
15 before completion of the proceedings, review of the
16 transcript [ ] was [ ] was not requested.
17
18   IN WITNESS WHEREOF, I have subscribed my name on
19 this date:
20
21
22
23
24   _____
25   Desiree Cooks, CSR No. 14075

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EXHIBIT 21

QCARM_7517717
Filed in Hard Copy

EXHIBIT 22

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

ARM LTD.,	
Plaintiff,	
v.	C.A. No. 22-1146 (MN)
QUALCOMM INC., QUALCOMM TECHNOLOGIES, INC. and NUVIA, INC.,	
Defendants	

REBUTTAL EXPERT REPORT OF DR. MURALI ANNAVARAM

FEBRUARY 27, 2024

HIGHLY CONFIDENTIAL – SOURCE CODE - ATTORNEY'S EYES ONLY

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I.   INTRODUCTION

1.   My name is Murali Annavaram. I have been retained to testify as an expert in this action on behalf of Defendants Qualcomm Inc., Qualcomm Technologies, Inc. (collectively, "Qualcomm"), and Nuvia, Inc. ("Nuvia") (together, "Defendants").   My qualifications and compensation are set forth in my previously submitted expert report in this matter on December 20, 2023 ("Opening Report"), which is incorporated by reference in its entirety in this report. As with my Opening Report, I am being compensated for my time at my standard consulting rate of $600, and my compensation is not contingent on any conclusions that I reach or opinions that I may reach.

2.   For this report, I have been asked to consider the analysis and opinions provided in the Opening Expert Report of Dr. Robert Colwell ("Colwell Report") and Opening Expert Report of Dr. Shuo-Wei (Mike) Chen on Qualcomm Source Code ("Chen Report"). I have reviewed Dr. Colwell's Report and Dr. Chen's Report and the materials in the attached Appendices and Exhibits.

3.   I have reviewed the Colwell Report and the Chen Report in the context of my experience, the materials cited in the reports, Nuvia and Qualcomm's development work, the incomplete ▮▮▮▮▮ Design (as existing at the time of the Nuvia acquisition),[1] and the SoCs that include: (1) one of the ▮▮▮ Family of Cores (i.e., the ▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮) and (2) the ▮▮▮ Family of Cores (collectively, I refer to the ▮▮▮ Family of Cores and the ▮▮▮▮▮ of Cores as the "Qualcomm Cores" or "Qualcomm's Cores")

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[1] When I use the phrase ▮▮▮▮▮ Design herein, I am referring to the design existing at the time of the Nuvia acquisition.

[2] When I use the phrase ▮▮▮▮▮ Core herein, I am referring to the Qualcomm Core that was worked on post-acquisition at Qualcomm under the Qualcomm ALA.

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(collectively, I refer to these SoCs as the "Qualcomm Product Designs" or "Qualcomm's Product Designs").[3] ██

██ When I refer to a Qualcomm Product Design for a particular one of the Qualcomm Cores, I may also sometimes refer to the SoC that incorporates one or more of that particular core. Each of Qualcomm's Cores and Qualcomm's Product Designs is represented by a respective Qualcomm Codebase and some of the design elements present in the code may also be described in ████████████████████████████████. The Qualcomm Codebase is, however, the authoritative source for information for any given Qualcomm Product Design.

4.   I expect to be called to provide expert testimony regarding opinions resulting from my analysis of the issues considered in this report, the materials that I have relied upon, and how I reached my opinions. If asked to testify about these issues, I may also discuss my own work, teaching, and publications in the field, knowledge of the state of the art in the relevant time period, and what certain technical terms are understood to mean in the field, including by those involved in the design of microarchitecture. I may rely on handbooks, textbooks, technical literature, my own personal experience in the field, and other relevant materials and/or information to explain relevant technologies, the state of the art in the relevant period, and the evolution of relevant technologies. I may also create demonstratives to further explain some of the discussion that appears in this report.

---

[3] I also discuss the ██████ SoC, which refers to the microarchitectural design outside of the CPU designed by Nuvia and Qualcomm. Qualcomm produced RTL for the ██████ SoC that I have reviewed.

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And, I may also discuss the source code that Qualcomm has made available for inspection that I have personally reviewed many times.

5.   I reserve the right to modify or supplement my opinions, as well as the basis for my opinions, in light of new positions taken by Arm of its experts, the nature and content of the documentation, data, proof, and other evidence or testimony that Plaintiff, ARM LTD. ("Arm"), or its experts may present, or based on any additional discovery or other information provided to me or found by me in this matter.

6.   I reserve the right to supplement the opinions in this report based on any subsequent testimony or facts revealed through discovery, as well as any subsequent reports produced by ARM's experts.

7.   To the extent any opinion in the Colwell Report or the Chen Report not mentioned below is directly or indirectly in conflict with any of my opinions expressed in this report, I disagree with Dr. Colwell and/or Dr. Chen, as applicable. Nothing in this report should be understood to be an agreement with any opinions expressed in the Colwell Report or the Chen Report except where I expressly state that I agree with Dr. Colwell or Dr. Chen.

II.   SUMMARY OF OPINIONS

8.   This section contains a summary of opinions I provide in this report.

9.   In my Opening Report, I discussed the Swap Out process that Qualcomm performed to replace Nuvia-sourced ARM Register-Transfer Level ("RTL") downloaded under the Nuvia TLA with Qualcomm-sourced ARM RTL downloaded under the Qualcomm TLA. In this Rebuttal Report, I address ARM's claims against Qualcomm and

3

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Nuvia related to the dispute concerning the Nuvia Architecture License Agreement ("ALA").

10.   Dr. Colwell states that he was "asked to analyze whether certain Qualcomm CPU cores incorporate technology developed by Nuvia under the [Nuvia ALA], ███████

███

███   ████████

███   Colwell Report

¶ 2 (emphasis added). Dr. Colwell has not shown that technology developed by Nuvia, or

Qualcomm, █████████████████████████████ delivered under the Nuvia ALA.

He has also not shown that (1) the ████████ Design (as existing at the time of the

Nuvia acquisition) █████████████████████ delivered under the Nuvia

ALA or (2) the Qualcomm Cores ███████████████████ delivered under

the Nuvia ALA.

11.   In answering the question he was asked to analyze, Dr. Colwell appears to

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███████████████████████████████████   Colwell Report ¶ 84.

12.   That is, Dr. Colwell opines that █████████████████████████

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████████████   *Id.*

13.   In offering his opinions, Dr. Colwell focuses on the Arm Architecture Reference Manual (the so called "Arm ARM"), which is a document published by Arm that includes within it an instruction set for the Arm Architecture and referred to as an instruction set architecture (ISA). The Arm ARM does not describe a processing element's (PE) microarchitecture or how to design one. The Arm ARM's purpose is to provide information about the Arm Architecture, and "is not intended to describe how to build an implementation of the PE [processing element]."[4] The Arm ARM describes various aspects of the Arm Architecture but not how to build a specific microprocessor that is compatible with the Arm Architecture. ARM makes this very clear in its own documentation as it explains the difference between architecture and microarchitecture, stating that "Architecture does not tell you how a processor is built or how it works. The build and design of a processor is referred to as micro-architecture. Micro-architecture tells you how a particular processor works."[5]

14.   Furthermore, Dr. Colwell appears to conclude that the entirety of the Arm ARM is included in "████████████," as that term is defined in the Nuvia ALA. I have been informed that Qualcomm and Arm disagree as to the meaning of "████████████,"

---

[4] Arm Ltd., Arm Architecture Reference Manual for A-Profile Architecture A1-38, (J.a 2023), https://documentation-service.arm.com/static/644a406baa78c007af74e6fd?token= (last visited February 21, 2024) (also produced at ARM_00011869).
[5] Arm Ltd., Learn the Architecture – Introducing the Arm Architecture 12, (2.1 2023) https://documentation-service.arm.com/static/64dcdf2a934840622b3496c9?token= (last visited February 4, 2024).

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including the scope of the deliverables listed in the Nuvia ALA Annex 1[6] and which

portions of the deliverables listed in the Nuvia ALA Annex 1 are captured by the definition

of "████████████." I have been informed that Arm's use of "███████████" is

broader than Qualcomm's.

15. ████████████████████████████████████

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16. ████████████████████████████████████

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[6] I understand that Nuvia entered into two Annex 1's in connection with the Nuvia ALA (September 27, 2019 and March 27, 2020). When I refer to Annex 1 herein, I am referring to the March 27, 2020 Annex. However, my opinions apply across both annexes.

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██ Dr. Colwell further opines that because the Oryon CPU corresponds to the ████ related Qualcomm Codebase, "the Snapdragon® X Elite platform of SoCs and Qualcomm Oryon CPU ██████████████ ████████████████████████████████" *Id.* ¶ 115. I disagree with each of these opinions. ██████████████████████████████████

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██████████████ Further, Qualcomm undertook substantial design and development of the ██████████ Core post-acquisition, and Qualcomm commenced the design and development work of the remainder of Qualcomm's Cores following the Nuvia acquisition, as I describe in Section VI. Still further, as I describe in Section VII, Dr. Colwell's opinion is not supported by Dr. Chen's analysis of the Qualcomm Codebases. Dr. Chen did not provide any analysis of the SOC codebase and, instead, limited his analysis to only a subset of files in what he calls the "██████████████████" In particular, in Section VII, I describe how Dr. Chen's source code analysis does not accurately calculate the similarities and does not demonstrate that any of the asserted similarities is derived from the ██████ ██████ Design (as existing at the time of the Nuvia acquisition).

19.   In this Rebuttal Report, I am responding to Dr. Colwell's analysis in the Colwell Report and Dr. Chen's analysis in the Chen Report. I am not a lawyer. █

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III.   BASIS FOR OPINIONS

20.   My opinions are based on my knowledge and experience in the technical areas at issue in this report and the materials that I have considered. My qualifications are summarized in Section II of my Opening Report.

21.   As part of my preparation for writing this report, I reviewed the materials listed in Appendix A to this report. These materials include, but are not limited to, the following: (1) Qualcomm's and Nuvia's development documents, microarchitecture specifications, and source code; (2) ARM's documentation including the ARM Reference Manuals, architecture documents and extensions; (3) license agreements and correspondence between the parties and copies of the documents described in this report; and (4) discovery responses and deposition transcripts.[7]

IV.   TECHNOLOGY BACKGROUND

A.   Processor Technology

22.   A System-on-Chip or SoC design places a variety of components such as processors, caches, memories, and input/output devices all on a single piece of silicon. Such a design offers both reduced latency for executing an application and reduced power consumption than a design in which the various components are placed on separate chips. One reason for improved SoC power efficiency and performance is that the components on the SoC can communicate with each other using on-chip wires that have lower resistance than off-chip pins. SoCs also enable integration of heterogenous technologies

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[7] I also incorporate by reference the Nuvia Agreements and Annexes and reserve the right to reference them and use sections as demonstratives.

such as central processing unit (CPU), graphics processing unit (GPU), volatile memory such as DRAM that holds application programs when they are executing, and non-volatile storage such as Flash memory that holds applications and other media files even when the device is turned off.

23.   One of the components typically included on an SoC is one or more Central Processing Unit (CPU) cores. Each CPU core may include additional components or blocks such as a data cache, an instruction cache, an Arithmetic Logic Unit (ALU), a Memory Management Unit (MMU), and a Floating Point Unit (FPU). A CPU may include only a single CPU core (called a single-core CPU or single-core processor) or may include multiple CPU cores (called a chip multiprocessor (CMP) or multi-core processor). The primary function of a CPU is to fetch, decode, and execute instructions to control and communicate with other components.

24.   A CPU is designed to process and execute instructions. The set of instructions that the CPU can execute are part of the instruction set architecture or ISA. The ISA can include simple instructions like "ADD" to add two numbers together, but may also include more complex instructions. While each instruction may perform only a simple operation, multiple instructions can be combined together in a program to perform complex operations that enable the development of the software commonly found on personal computers and mobile devices.

25.   Each instruction supported by the CPU is defined in the ISA in terms of what that instruction does (e.g., a logic operation, a data transfer operation, or a jump operation), in terms of where that instruction obtains its operands and stores its results (e.g., a memory address or a register), and in terms of the format of the instruction (e.g., its length

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and the meaning of its fields). Everything included in the ISA is visible to a programmer who is using those instructions to write a program to be executed by any CPU designed to support that ISA.

26.   Although the ISA specifies the instructions that are supported by a CPU, the ISA does not specify the design of that CPU. There are many different ways to implement an ISA, and none of those different ways is defined by or required by the ISA. The instructions include opcdoes represented by binary that lacks creativity. For example, Intel processors and AMD processors are two different implementations of the commonly-recognized x86 ISA. A particular implementation of an ISA is referred to as a microarchitecture, and different microarchitectures can vary in such things as power consumption and performance based on the goals and details of its design.

27.   The value of the ISA arises from the value that software and hardware programmers invest into creating their own, unique programs and CPUs that operate using the ISA interface. If the designer of the CPU complies with the ISA, then a program written with those instructions can be executed by the CPU. As additional software and hardware is developed using the ISA, the benefits of the ISA continue to grow as a more established and expansive ecosystem is created.

B.   RTL

28.   RTL describes the implementation of the CPU's microarchitecture. RTL design is a digital design methodology that focuses on the transfer of data between registers within a digital system. It serves as an abstraction level between the high-level behavioral description of a system and its physical implementation in hardware. At the Register-

Transfer Level, designers describe the behavior of the system in terms of registers, data flow, and control signals.

29.   The RTL can be created manually using a Hardware Description Language (HDL) such as Verilog or it can be created automatically from a higher-level language using an RTL synthesis tool. After the RTL representation is completed, many additional steps are needed, such as wiring place and route, and verification. Once all these steps are completed the RTL specific design can be used to create an actual physical device.

30.   RTL may be organized into groups of code referred to as "modules," with each module likewise organized into smaller groups of code referred to as "submodules." Organizing the RTL into modules and submodules improves the efficiency in managing large projects by allowing code to be modularized and re-used in different aspects of the projects. For example, the RTL modules for complex functions implemented in a CPU can be treated as abstract boxes with input and output pins. Hence different module developers can easily interface without knowing the details of the module design.

31.   Verilog has many things in common with regular programming languages like C or Fortran. For example, a module is, conceptually, very similar to a subroutine. However, the behavior of a Verilog program is generally dictated by the way signals are routed across connected modules rather than by the order of code that appears within the Verilog program.

32.   For a simple example of RTL language, consider a D (Delay) flip flop that transfers an input value to an output on the falling edge of a clock signal. This is a common component in digital logic circuits, like CPUs. The flip flop can be used to temporarily

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store data during CPU operation. The behavior of such a component could be described

with RTL as follows:

```
Module Dff(q, clock, data);
output    q;
reg       q;
input     clock, data;

initial
q=0;

always
@(negedge clock) #1 q=data;
endmodule
```

33.   The "always" statement in that RTL description indicates that when the

clock goes from high to low (i.e., on a falling or negative edge) the output register "q" is

assigned the input value "data" after a delay of one time unit.

34.   The use of RTL in the design of a CPU provides numerous advantages

including ease of development of the processor using a high-level programming

abstraction, much like writing software using C/C++ to accomplish an application task.

The hardware designers do not need to worry about how the digital gates, such as AND

and NOR gates, are implemented in a particular process technology node.

35.   A second advantage provided by RTL is structured design validation in

which the designers are able to simulate and test individual modules separately and then

test the interfaces between modules and submodule to achieve a hierarchical testing

approach. These tests must go beyond simply testing the functionality of an instruction

and instead test the various detailed microarchitectural interactions. Such structured testing

allows the designers to identify and correct problems in the microarchitecture much earlier

in the design process and with much less cost than would be incurred later in the process.

36.   A third advantage provided by RTL is modularity. Designers can create libraries of RTL components that can be easily reused across an entire design. For example, the flip flop described in the example RTL code above may be a defined module that is re-used throughout several blocks of an SoC. These reusable blocks can be easily integrated into new designs, promoting design reuse, reducing development time, and enabling faster prototyping and system assembly.

C.   **Overview of Computer Systems**

37.   Computer systems are segmented into various levels of abstraction.

38.   The top layer is the application software. It is the layer that users are most familiar with (e.g., a word processor, calculator, video player, or any other program). Programmers typically write application software in high-level programming languages like C++ and Java.

39.   The Operating System ("OS") interfaces between an application and the hardware, and it performs operations such as allocating storage and memory, handling basic input and output operations, and enabling multiple applications to use the same microprocessor simultaneously. Examples of OSs include Windows, Mac, and Android.

40.   The next layer of the stack is the ISA. ISA refers to the instruction set, which includes the list of instructions that a compatible processor may execute, operands formats, and a memory model. Operands are objects upon which an instruction operates. For example, in the instruction "a = b – c", a, b, and c are considered operands and subtraction (-) is considered the operation. Not all instructions have operands. Examples of ISAs include Arm, x86, RISC-V, and MIPS.[8]

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[8] Arm Architecture Reference Manual for A-Profile Architecture, Issue J.a., *supra* note 4; Dave Jaggar, Arm Architecture Reference Manual (2d ed. 2001); RISC Machs. Ltd. (ARM), Arm Architecture Reference Manual,

41.   The next layer of the stack is microarchitecture. Microarchitecture is the design of a computer's processor in which an engineer specifies how the processor executes instructions received from the application . For the same ISA there may be many different microarchitecture designs with different characteristics.   Different microarchitecture designs may be made with different choices regarding trade-offs of performance, power, cost, and complexity, allowing designers to design microprocessors optimized for particular types of markets. A microprocessor built for a server data processing system may be vastly different from a microprocessor built for mobile systems, even for the same ISA. The microarchitecture can be used to synthesize logic circuitry according to the designed microarchitecture.

42.   A designer designs a microarchitecture in a language such as Register Transfer Language ("RTL"), which I described in my Opening Report. Once written in RTL, a series of hardware synthesis and design tools may synthesize the RTL into the actual circuits and gates that are ultimately fabricated onto a chip.

D.   Instruction Set Architecture

43.   In this section, I introduce the concept of instructions and ISAs, including opcodes and field registers.

1.   The role of an instruction is to specify the hardware functionality an application can use

44.   An ISA includes a set of instructions that specify how applications interface with a microarchitecture to execute operations. The instructions are represented in binary format.   Each instruction represents an operation, such as an ADD or MULTIPLY

(B 1996); Gerry Kane and Joe Heinrich, MIPS Risc Architecture (2d ed. 1991); Andrew Waterman, et al., The RISC-V Instruction Set Manual Vol II (2021).

operation, as a series of binary bits. The instruction may include a set of source operands and a destination operand to specify the data for the operation. This binary representation of instructions is known as *machine language*.

45.   Operands may come from memory, registers, or the instruction itself. For example, an instruction such as an ADD instruction may contain information on the location in memory of the two numbers to add. A programmer could write this instruction in a lower-level programming language, such an *assembly language,* as "ADD A,B", where A and B are the operands, and an assembler would convert it into machine language (the binary code of an ADD operation). In general though, software programmers use higher-level programming languages such as C, C++ or Java that can be put by a compiler into assembly language and subsequently to machine language. For example, a C program is compiled into assembly language and then assembled into binary machine language.

2.   An ISA forms an abstract interface between the hardware and software of a computing device

46.   The ISA allows a software programmer to focus on operations separately from the microarchitecture that delivers the actual results within a given power, performance or cost constraints.

47.   Each instruction in an ISA has an associated operation code, referred to as an "opcode", which is the binary string that uniquely identifies instructions. A microprocessor "decodes", in other words recognizes, the representations of the instructions to get the opcode. The microarchitecture decodes the opcode to determine the operation represented in the opcode and generate control signals that carry out the operation according to how the designer designed the microarchitecture.

48.   Any microprocessor design compatible with the Arm ISA must recognize the instructions (or "vocabulary") of the architecture in order for the same application to produce the same results across different microprocessors designed with different microarchitectures. An example definition of an instruction specified as a certain sequence of 1's and 0's is shown below[9]:

ADCS

Add with Carry, setting flags, adds two register values and the Carry flag value, and writes the result to the destination register. It updates the condition flags based on the result.

31 30 29 28	27 26 25 24	23 22 21 20	16	15 14 13 12	11 10 9	5 4	0
sf 0 1 1	1 0 1 0 0 0 0	Rm		0 0 0 0 0 0	Rn	Rd	

op S
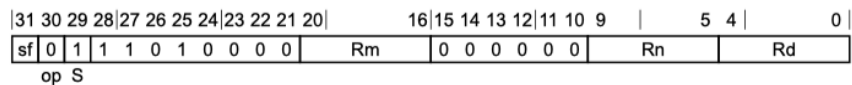
49.   In order for an application to be executed by different microarchitectures supporting the same ISA, the microprocessor must recognize this sequence of instruction bits as an opcode indicating an addition with carry operation that must be performed with the source operands specified in the Rm, Rn fields and putting the result in register Rd.

50.   In the microarchitecture for a microprocessor, the opcode is decoded into control signals. The number of and type of control signals is designed by the microarchitect to correspond to the portions of the microarchitecture that carry out the operation performed by the instruction. The decoding thus designed is unique to each microprocessor's microarchitecture. The opcode itself, reflected in the ISA, is decoded but the output of the decoder is a specific sequence of 1's and 0's that activate the various microarchitectural structures that are specific to a particular processor design.

51.   A designer is free to design the microarchitecture in any number of ways to perform the operation indicated by the opcode. A microarchitecture design can fail to

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[9] ARM v8 C6.6.2.

achieve success in the market, regardless of any characteristics and benefits thereof of the architecture. For example, a designer may make poor choices in the trade-offs involved in the microarchitecture and as a result not be successful in the target market despite being compatible with a certain ISA. Thus, the success of a company's microprocessor has to do with the designer and whether the microarchitecture design provides better performance/power/features over competitors.

52.   Dr. Colwell discusses companies such as Apple and Alphabet as multi-trillion dollar industries. Colwell Report ¶ 20. The success of these companies is a complex function of many market demands and product innovations, most of which are not all related to microprocessors.

53.   Similarly, Dr. Colwell suggests that the success of the Internet, smartphones, and the like is based on computers and processors becoming fast enough and inexpensive enough. *Id*. ¶ 21. However, the success of computer technologies is a result of efforts from engineering teams working across a wide range of challenges, including challenges separate from microprocessor development and work performed before the existence of ARM. For example, the development of wireless communications was a major factor to the success of the Internet and mobile devices.

54.   Many ISAs, such as Intel's x86 ISA, IBM's Power ISA, the MIPS ISA, or the RISC-V ISA, provide similar instructions as one another. For example, the opcode ADD in the ARM ISA specifies that values stored in two registers must be added together. The same instruction exists in the RISC-V ISA and the Intel x86 ISA.

55.   Dr. Colwell claims that ARM "explicitly aimed to enable compatible implementations that emphasized good performance at outstanding power efficiency." *Id*.

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¶ 27. Although many ARM-compatible microprocessors do target power efficiency, rather than any substance or teaching in the ISA, the power efficiency is obtained through significant engineering effort in the design and fabrication of the microarchitecture of the microprocessor, a process which I describe in other sections of this Report. Indeed, Dr. Colwell describes the same when he notes that a microarchitecture can "optimize[] performance above all else, including at the expense of high power and high product cost" or can be "optimized for low power and long battery lift, as required by mobile platforms such as tablets, smartphones, and laptops." *Id*. ¶ 39.

E.   Microarchitecture

56.   While the ISA specifies instructions that an application programmer can use to interface with the microprocessor, the microarchitecture defines how the operations are carried out and the microarchitecture is designed to fit a particular constraint such as power/area, and the market requirements. The microarchitecture of a processor is designed in accordance with the needs of a market segment a processor is targeted for. There are also constraints on cost, power, performance, thermals, area, and complexity a designer has to grapple with in designing a microarchitecture.

57.   For example, one of the microarchitecture design choices is to decide on the pipeline stages implemented in a core. A pipelined execution splits the work associated with an instruction into multiple smaller work chunks. And each smaller chunk of work is done using a single pipeline stage and each pipeline stage is generally completed in a single clock cycle. Processor microarchitects may choose deeper pipelines for high frequency execution or shallower pipelines for reducing design complexity.

58.   Microarchitects may also choose to implement in-order pipelined execution or out-of-order pipelined execution.   In out-of-order processors the execution of instructions can proceed in an order that is different than the compiler generated code order. Out-of-order (OOO) execution allows a newly arriving instruction to start its execution even if there are some older instructions waiting in the pipeline for their source operands. This choice of OOO or in-order execution is a design decision made by the microarchitect.

59.   OOO execution allows faster execution of a program by allowing instructions to execute as soon as their source operands are available, without waiting for the precise order of the code generated by the compiler. But, the designer has to handle significant challenges posed by OOO execution none of which is defined in any ISA document, such as the Arm ARM.

60.   One such challenge is conditional execution. Applications routinely insert conditional execution statements. For example, a programmer may want to add two numbers *if* the two numbers are positive. Thus a condition must be verified before the addition operation can be performed. Waiting for the verification of the condition slows down the program. Hence the microarchitect may choose to ***speculatively*** execute the addition operation. But such speculative execution has to be guided by some confidence that the values used in the addition are positive. Such a confidence mechanism must be designed by the microarchitect.

61.   Branch predictor hardware is built for this purpose to enable a more informed guess on whether the condition is going to be true or not. If the guess is wrong, then the microarchitect has to design additional microarchitecture structures to remove the effects of wrongly executing the instruction, a process called branch misprediction

handling.   Both   branch   predictors   and   misprediction   handling   structure   are microarchitectural choices that are made by the designer.

62.   Another challenge in OOO execution is the memory hierarchy.   When executing instructions, the source operand data must be brought as close to the execution units as possible.   While all the source operands are available in large memory chips accessing data from such large memory chips is slow compared to the speed of the instruction execution.   Hence, waiting for data to be fetched from memory is not a viable option.

63.   To tackle the memory latency challenge, microarchitects design small amounts of fast memory, called caches, closer to the processor.   These cache memories allow for temporary storage of a small sample of application data.   It is the microarchitect's responsibility to determine what sample of data is to be brought in, and for how long it should stay in the cache before it is replaced by another data sample.   These policies and procedures are complex, and a microarchitect designs these caches.

64.   In fact, microarchitects design hardware structures called prefetchers that speculatively bring data from distance memory into nearby caches.   These prefetch hardware structures must track past behaviors of the program, in specialized hardware structures, and determine what sample of data must be prefetched into the cache.   That way, at a future time, if this data is requested by the application that data is quickly accessed from the cache, rather than going to the slow memory.   It is also possible that the data that is prefetched may be wasted if it is not later used by the application.   Hence, the microarchitect has to carefully consider the cost of speculatively bringing data, for example

the cost of wasted power. Microarchitecture for prefetching is not described in an ISA document, such as the Arm ARM.

65.   An application has many instructions with dependencies. One instruction may generate data used by another instruction. For example, a store operation may store data to cache that may be later loaded by a load operation. Thus, OOO execution has to consider the dependency order and must strictly respect the data dependency requirements. Yet again, the microarchitect must deal with this issue of when to reorder instructions without causing program inaccuracies. The microarchitecture may design new types of dependency predictors, such as load/store dependency predictors, to handle such a situation. Microarchitecture for predictors is not described in ISA documents such as the Arm ARM.

66.   Some market segments such as datacenter servers exhibit workloads that cause designers to choose to implement large number of homogeneous cores on a chip. Large homogeneous multicore processors have been correctly described as an "enabling technology for large application domains with abundant threads, such as computer graphics, scientific/engineering computing, database management, and telecommunication services."[10]

67.   For a mobile market segment, the microarchitect may choose to implement heterogenous multi-core processors where each core may be optimized for a different type of application. For instance, a web browsing application on a mobile phone may require a relatively moderate performance core, while a gaming experience may require high performance core.   Thus, the microarchitect has to design the type and level of

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[10] Dubois, et al., Parallel Computer Organization and Design xi, (Cambridge Univ. Press 2012).

heterogeneity to incorporate into a processor design, and microarchitecture heterogeneity is not described in an ISA document, such as the Arm ARM.

68.   To summarize, whereas an ISA document such as the Arm ARM specifies instructions to execute and the structure of the operands, the ISA does not provide the microarchitecture, let alone the step-by-step methods utilized by the control and datapath, all of which designers accomplish through innovation and creativity when designing the microarchitecture. An ISA document, such as the Arm ARM, does not specify or provide microarchitecture for different power, performance, and other requirements of the intended use case.

69.   When a binary bit pattern of an instruction is received by the processor, the instruction may be stored into caches for efficiently accessing instructions without having to repeatedly access main memory. The caching policies and cache management is a microarchitecture detail of the core that is not guided by the Arm ARM. Once the instructions are cached, the instructions are then accessed and decoded. The decoder is a hardware component, developed by the microarchitect, that is designed to read the instruction and decode the representation in the instruction to identify the operation requested by the application. The decoder's output is a set of control signals, potentially hundreds or thousands, that are designed to match the microarchitecture of a particular core and differ from design to design. For example, the decoder may generate the appropriate read and write port enable signals to read and write the data from the registers. The number of ports and their access latencies are all part of the microarchitecture, and not described in the Arm ARM. The outputs generated from the decoder are thus driven by the microarchitecture of the core.

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F.   From Microarchitecture to Silicon

70.   The microarchitecture that I described above is usually written in a hardware description language, such as Verilog or VHDL (e.g., the RTL code I described in my Opening Report). These hardware descriptions have to be eventually synthesized into circuits and gates that can be implemented in silicon (e.g., as a physical chip). There are tools that automate this process to some extent. The designers still have to fine tune the outcomes provided by these tools to get the best results. The final gate level design produced by these tools results in a file called Netlist file which will be readied for fabrication, where the physical silicon chip is produced with the designed microprocessor.

71.   After fabrication, the microarchitecture is represented in the physical structures on a physical chip that includes transistors, wires, and other components built on a substrate, typically silicon. For this reason, the term "silicon" is used in the CPU industry to refer to physical chips produced by a microarchitect, whether Nuvia or Qualcomm. Dr. Colwell did not discuss any physical chips, and thus I have not analyzed any physical silicon as part of the preparation of my Rebuttal Report. I have been informed that, as described by Christin Cong Tran, ███████████████████████████ ██ that Arm does not believe that physical silicon chips created by Qualcomm are covered by the ███████ termination obligations. Tran Dep. Tr. at 164:5-166:8.

V.   BACKGROUND FACTS AND TIMELINE

72.   In this section, I will discuss background facts relevant to this report including the parties, nature of the dispute, and Nuvia's Architecture License Agreement ("ALA") with ARM. I will further provide a timeline outlining facts relevant to this report.

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A.   The Parties

1.   Qualcomm

73.   Founded in 1985, Qualcomm is a technology company that develops and manufactures integrated circuit products (i.e., chips) and licenses its technology. Qualcomm has been a "global leader in the development and commercialization of foundational technologies for the wireless industry, including 3G (third generation), 4G (fourth generation) and 5G (fifth generation) wireless connectivity, and high-performance and low-power computing including on-device artificial intelligence (AI)."[11]

74.   Today, Qualcomm's chips are found in mobile phones, laptops, virtual and augmented reality products, autonomous driving and digital cockpit solutions, wearables, and smart home products, among others.[12]

75.   Qualcomm's Snapdragon products are highly integrated, system-based solutions that include the Snapdragon mobile, compute, sound and automotive platforms. Each platform consists of microprocessors and wireless connectivity capabilities, including Qualcomm's cellular modem that provides core baseband modem functionality for voice and data communications, non-cellular wireless connectivity (such as Wi-Fi and Bluetooth) and global positioning functions. Qualcomm's Snapdragon microprocessor operations include artificial intelligence ("AI") / neural processing unit ("NPU"), CPU, security, graphics, display, audio, video and camera. Qualcomm's CPUs are designed to deliver high levels of compute performance with optimized power consumption. Qualcomm Hexagon NPUs are designed to support a variety of AI processing tasks for superior performance-per-watt. Qualcomm Adreno graphics processing units are designed

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[11] Qualcomm Inc., Annual Report (Form 10-K) at 6 (Nov. 1, 2023).
[12] Products, Qualcomm, https://www.qualcomm.com/products (last visited Feb. 26, 2024).

to deliver high quality graphics performance for visually rich 3D gaming and user interfaces. And, Qualcomm also designs and supplies supporting components, including the RF transceiver, PM (power management), audio, codecs, speaker amps and additional wireless connectivity integrated circuits.

76.   The figure below is a simplified block diagram of a Snapdragon SoC. The microprocessor is the portion of the SoC that may include CPUs (labeled as Kryo 385 CPU)[13] but the SoC also includes many other components (illustrated as GPU for driving visual displays and games on the device, ISP for processing camera data to take pictures, etc.). The CPU(s) in an SoC are only a small portion of the functionality provided by the SoC, and each of the components may provide a feature or benefit of desire to a user. For example, photography on a computing device is an important consideration to a user, and that photography is supported by the ISP. As another example, wireless communications on a computing device is an important consideration to a user, and that wireless communications is supported by the modem. Each of these blocks involve significant engineering effort on their own, in addition to significant engineering effort in combining the blocks into a single SoC.

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[13] The illustration inserted below references a Kryo 385 CPU. This illustration is of a prior Qualcomm SoC that is part of the Qualcomm Snapdragon 845 Mobile Platform. The Kryo 385 CPU included in that platform is a CPU that includes a microarchitecture from the ARM Cortex family. The Qualcomm Product Designs I describe throughout this Rebuttal Report are compatible with the Arm ISA but different in design than the Kryo 385 CPU and the ARM Cortex.
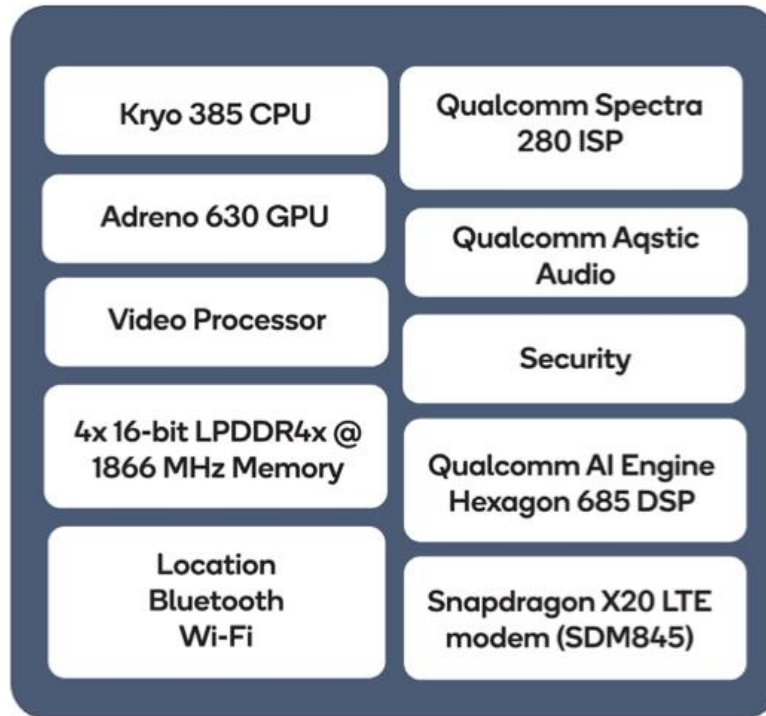
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2.   Nuvia

77.   NUVIA Inc was founded by Gerard Williams III, Manu Gulati, and John Bruno in early 2019 to design a data center processor chip that is faster and more power-efficient than current offerings.[15] Nuvia targeted customers that run massive data centers and primarily use chips from Intel Corp and Advanced Micro Devices Inc.

78.   Prior to co-founding Nuvia,[16] Gerard Williams III was a Senior Director at Apple and Chief CPU Architect for nearly a decade with responsibilities for a range of leading-edge CPUs and SoCs across a broad array of devices. Before joining Apple, Mr. Williams spent over 10 years at ARM, as an ARM Fellow, and serving on the ARM

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[14] Qualcomm, Qualcomm SDM845 / Qualcomm SDA845 SOCs at 2 (2020), https://www.qualcomm.com/content/dam/qcomm-martech/dm-assets/documents/sdm-sda845-product_brief_87-pu778-1.pdf.

[15] Steven Nellis, *Nuvia, Founded by Ex-Apple Execs, Raises $240 mln for Data Center Chips*, Reuters, Sept. 24, 2020, https://www.reuters.com/article/idUSL2N2GL032.

[16] Gerard Williams III, LinkedIn, https://www.linkedin.com/in/gerard-williams-iii-27895aa (Feb. 27, 2024).

Architectural Review and Technical Advisory Boards. While at ARM, he served as a technical advisor for the ARM architecture and CPU development to many key ARM partners. Mr. Williams began his career with tenures at Intel and Texas Instruments.

79.   Prior to co-founding Nuvia,[17] Mr. Gulati was the lead SoC Architect for consumer hardware at Google, playing a key role in defining the company's silicon and product roadmaps. Before joining Google, Mr. Gulati spent eight years at Apple as the lead SoC architect responsible for numerous Apple leading-edge mobile SoCs across a range of devices. Before joining Apple, Mr. Gulati spent nearly a decade at Broadcom holding a range of senior SoC engineering roles. Mr. Gulati started his career at AMD and 8x8 and has over 58 issued patents to date.

80.   Prior to co-founding Nuvia,[18] Mr. Bruno was a System Architect at Google, driving such areas as SoC definition and competitive performance and power analysis. Before joining Google, Mr. Bruno spent five years at Apple in a similar role in the company's platform architecture group where he founded Apple's silicon competitive analysis team. Mr. Bruno started his career in 1996 as an ASIC designer at ATI Technologies Inc. where he climbed the ranks to become the ASIC team leader responsible for multiple mobile GPUs and integrated chipsets. After AMD's acquisition of ATI, Mr. Bruno became the Chief Engineer for the Trinity Fusion APU.

81.   Nuvia sought to tap its founders' experience building powerful chips for battery-powered devices.[19] Qualcomm publicly announced that it would be acquiring

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[17] Manu Gulati, LinkedIn, https://www.linkedin.com/in/manu-gulati-283346 (last visited Feb. 27, 2024).
[18] John Bruno, LinkedIn, https://www.linkedin.com/in/john-bruno-p-eng-88616a1 (last visited Feb. 27, 2024).
[19] Steven Nellis, *Former Apple Chip Executives Found Company to Take on Intel, AMD*, Reuters, Nov. 15, 2019, https://www.reuters.com/article/us-nuvia-tech/idUSKBN1XP19V/?il=0

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Nuvia on January 12, 2021,[20] and Qualcomm publicly announced that it completed the acquisition on March 15, 2021. The ▇▇▇▇▇▇▇ Design (as existing at the time of the Nuvia acquisition) was a work in progress and was not ▇▇▇▇▇▇▇▇▇▇▇▇▇▇▇ nor a product ready for use. The ▇▇▇▇▇▇ Design included the starting development of a microprocessor core intended for server markets. As I describe elsewhere in this Rebuttal Report, the ▇▇▇▇▇▇ Design (as existing at the time of the Nuvia acquisition) was not ▇▇▇▇▇▇▇▇▇▇▇▇▇▇▇▇▇

3.   ARM

82.   Arm is a semiconductor and software design company, whose primary business is the design of central processing unit (CPU) cores that implement the ARM architecture family of instruction sets. ARM also designs other cores such as graphics processing units (GPUs) and others. Companies often licenses CPU core designs from Arm to manufacture and integrate the core into their own System on chip (SoC) with other components such as GPUs (sometimes their own and sometimes the Arm Mali) and modem/radio basebands (for mobile phones).

83.   ARM also grants licenses that allow licensees to develop their own highly customized CPU designs that is compliant with the Arm ISA. Arm's claims against Qualcomm relate to Qualcomm's customized designs, not Arm designs.

B.   Nature of Dispute

84.   In this section, I will discuss my understanding of the dispute between Qualcomm and Arm as informed by Qualcomm's attorneys. I understand that in its

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[20] Qualcomm, Qualcomm to Acquire Nuvia (Jan. 12, 2021),
https://www.qualcomm.com/news/releases/2021/01/qualcomm-acquire-nuvia

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complaint, Arm has brought a breach of contract claim against Qualcomm.[21]   D.I. 1

(Compl.) at ¶¶ 58-69. When Qualcomm announced its intent to acquire Nuvia, both Nuvia

and Qualcomm had their own respective ALA in place with Arm.   *Id.* ¶ 21;

QCARM_0337857; QCARM_0337839.

85.   Specifically, on September 27, 2019, Nuvia and ARM entered into an ALA

and a Technology License Agreement ("TLA").[22] Nuvia and ARM entered into an Annex

1 for both the ALA and TLA on September 27, 2019,[23] and then on March 27, 2020,[24]

Nuvia and ARM entered into another Annex 1 for both the ALA and TLA. My report

focuses on topics related to the Nuvia ALA in response to Dr. Colwell's and Dr. Chen's

opinions, and I have been informed that ARM's claims are specific to the Nuvia ALA.

86.   I understand that ARM terminated the Nuvia ALA on March 1, 2022.

Compl. ¶ 39. ARM claims that it "is entitled to specific performance requiring Defendants

to comply with the Nuvia ALA's termination provisions, including ceasing all use of and

destroying any technology developed under the ALA." *Id.* ¶ 68.   The Nuvia ALA

termination provision, ▌▌▌▌▌▌, states as follows:

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[21] I understand that ARM has further alleged counts of Trademark Infringement and False Designation which are not relevant to the discussion in the report.
[22] QCARM_0337839; QCARM_0338297.
[23] ARM_00003097; QCARM_0275743.
[24] QCARM_0315570; QCARM_0339326.

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QCARM_0337839 at 852.

87.   I am not an attorney and understand that ARM and Qualcomm disagree over the meaning of ███████████████

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[25] For convenience, I will adopt the same naming convention to reference this document throughout my report.

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[28] I am not reproducing here direct quotes from the Nuvia ALA supporting Qualcomm's position, but I incorporate them by reference and reserve the right to use these texts and use them as demonstratives at trial.

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90.

C. Timeline

91. I have been provided the following timeline of events:

- On May 30, 2013, Qualcomm, through its affiliate, entered into an Amended and Restated ALA and Amended and Restated Agreement with Arm. QCARM_0337857. According to this ALA, Qualcomm's and ARM's original ALA was dated September 29, 2003. *Id*. Qualcomm through its affiliate entered into a Technology License Agreement ("TLA") with Arm effective as of May 30 2013 as well. QCARM_0343533. According to this TLA, the original TLA was dated September 30, 1997. *Id*. This TLA has remained in place and effective through the current day. On September 27, 2019, Nuvia and Arm entered into an ALA and TLA. QCARM_0337839; QCARM_0338297. Nuvia and Arm entered

into an Annex 1 for both the ALA and TLA on September 27, 2019. ARM_00003097; QCARM_0275743. On March 27, 2020, Nuvia and Arm entered into another Annex 1 for both the ALA and TLA, which changed some of the listed deliverables, and I have been informed the 2020 Annex 1 is the controlling Annex for the Nuvia ALA, which Dr. Colwell appears to understand as the controlling Annex as well. QCARM_0315570; QCARM_0339326.

- On January 13, 2021, Qualcomm publicly announced its intent to acquire Nuvia. QCARM_0002470.

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- On March 15, 2021, Qualcomm publicly announced it acquired Nuvia.[29]

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- On March 1, 2022, ARM terminated the Nuvia ALA and TLA. ARM_00037427.

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[29] Qualcomm, Qualcomm Completes Acquisition of NUVIA (Mar. 15, 2021), https://www.qualcomm.com/news/releases/2021/03/qualcomm-completes-acquisition-nuvia (last visited February 27, 2024).

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VI.   THE ████████████████ **DESIGN AND QUALCOMM PRODUCT DESIGNS ARE NOT** ███████████████████████████████████████

92.   For context regarding Dr. Colwell's and Dr. Chen's analysis, it is helpful to consider what they focus on. As I discussed above, the microprocessor is one of many modules found within an SoC. The microprocessor itself includes multiple modules, and a microarchitect, among other things, designs the different modules by writing RTL code to perform an operation in such a way as to meet criteria related to the goals for the design (which are, for example, indicated by the needs of the targeted market).

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94.   The SoC of the ███████████ Design is shown below:
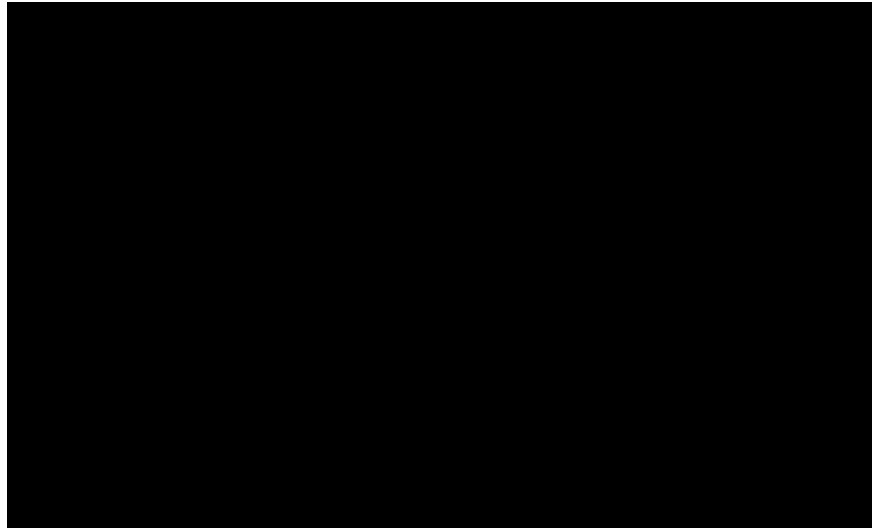
QCARM_2418347 at -360.

95.   ███████████████████████████████████████

96.   ███████████████

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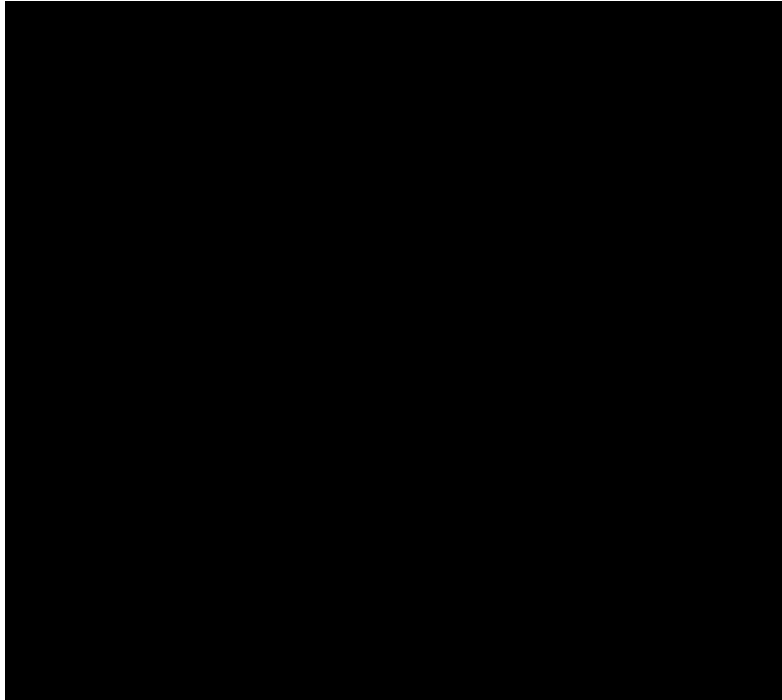
QCARM_0357004 at -008.

97.
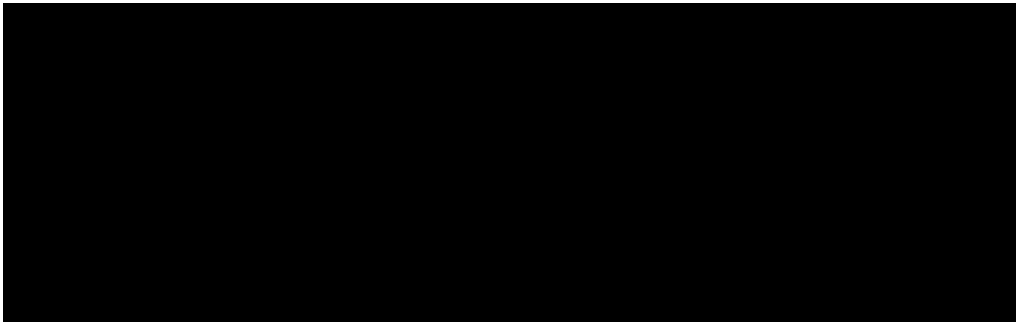
Id. at -020.

A.   **The Arm ARM does not define a microarchitecture**

98.   Market needs that guide product requirements serve as the basis for microarchitecture design.   ARM itself has characterized the Arm ARM as simply

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describing "what functionality the software can rely on the hardware to provide."[30]   A microarchitecture's design involves choices about hardware components, their arrangement, and operational methodologies. In fact, microarchitectures that share the same architecture can differ significantly.

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100.   As described in greater detail below, a licensee's (such as Nuvia or Qualcomm) design team builds their *own* microprocessors that executes operations that can be accessed through the software interface I describe elsewhere that is the Arm ARM.

       1.   **Microarchitectural design choices greatly impact product attributes and hence product use cases**

101.   A microarchitecture's design takes price, performance, and power requirements into consideration. While two microprocessors may use the same ISA, the design of each microprocessor could look and function very differently due to the innovations and design choices that designers implement. These design choices are usually governed by the requirements of the product in which the microprocessor is used. For example, a CPU for a smartphone may be designed to use less power than a CPU in a data center, even when they implement the same architecture.

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[30] Arm Ltd., *supra* note 5, at 9.

102.   For example, a processor design for a personal mobile device, such as a smartphone, may focus more on power, media performance and responsiveness, whereas processor design for a server (which is typically a plugged-in device) would be more focused on data throughput to support multiple applications and/or users.

2.   Key product characteristics depend primarily upon microarchitecture design choices, and not upon the choice of ISA

103.   The differences in required product performance driving different microarchitecture design choices are independent of the choice of ISA. As an example, two processors with the same ISA but different designs are the AMD Opteron and the Intel Core i7. Both processors implement the x86 instruction set, but they have very different pipeline and cache organizations. I will discuss pipeline and cache organizations in further detail in later sections.

104.   The Arm ARM does not provide a microarchitecture. Knowing that an ADD operation needs to add two numbers stored in registers, the functional description, does not say anything about how fast the ADD operation must be performed, how much power that ADD operation is allowed to burn, how the circuit design of the adder is implemented, how many transistors are needed to implement the ADD operation, how to read the data from the registers and bring them into the adder module. Once an Arm instruction is decoded the difficult work of achieving the efficient processor design is left to the designers. That is in fact the reason why Apple's M1 chip has successfully been adapted into MAC computers. It is the innovations in the microarchitecture that create the value and product differentiation. For example, the same software application may run

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slowly on one microarchitecture and quickly on another, or it may consume more power while running on one than the other.

105.   As one example in the Arm ARM, Dr. Colwell states that the Arm ARM provides information such as the "number, types and any special aspects of the general register set."   Colwell Report ¶ 59.   However, Dr. Colwell did not consider that Qualcomm's complex out-of-order processors use the concept of register renaming where architectural registers are mapped to the physical registers on the chip.   Throughout the execution of the instructions it is the physical registers that are read, written and tracked.

106.   As another example, I disagree with Dr. Colwell that the Arm ARM specifies the "memory hierarchy design, including caches, write buffers."   *Id.*   The Arm ARM does not specify the cache configuration, such as the size of the cache in bytes, the width of each cache line, the number of such cache lines, the associativity of the cache.

107.   Processors that are compliant with the ARM ISA can have a variety of microarchitectures, each balancing performance, cost, and complexity differently.   Despite their internal designs being vastly different, they all execute the same programs.   The table below presents a range of processors that all utilize the Arm v8.2-A ISA, but are designed for very different use cases, which in turn, leads to different microarchitecture designs.

Core	Arm ISA Version	Use Case
Neoverse N1[31]	v8.2-A	Infrastructure/Server Applications
Cortex-X1[32]	v8.2-A	Google Tensor (SoC for Pixel), Exynos 2100 (Samsung SoC), Snapdragon

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[31] Arm Ltd., Arm Neoverse N1 CPU (2019), https://www.arm.com/-/media/global/products/processors/N1%20Solution%20Overview.pdf?rev=1cf46d423a6b4995809c94b14109b805&revision=1cf46d42-3a6b-4995-809c-94b14109b805.

[32] Arm Ltd., Arm Cortex-X1 Core Technical Reference Manual (r1p2 2023), https://documentation-service.arm.com/static/64bfd6eedf6cd61d528c8a20?token=.

Core	Arm ISA Version	Use Case
		888 (for smartphones, tablets, smartwatches, laptops)[33]
Neoverse E1[34]	v8.2-A	Edge Computing
Cortex-A65AE[35]	v8.2-A	Automotive Applications like Advanced Driver-Assistance Systems[36]

Exemplary ARM Processors & Use Cases

108.   The uniqueness and effectiveness of a processor's microarchitecture generally become evident to computing device purchasers via the performance of the computing device.

109.   There are different performance results from two different microarchitecture implementations even when holding fabrication and ISA constant.

110.   Because of the impact that differences in microarchitecture can make, microarchitects need to select the microarchitectural techniques carefully based on the domains they are targeting. In Section VI, I describe these techniques in more detail, and explain how they impact the characteristics of processors like performance. As I have described above, very different microarchitectures for a microprocessor can be designed while still maintaining compatibility with an ISA.

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[33] Saurabh Pradhan, *Arm Cortex-X1C: Scalable Innovation for Laptop and Desktop*, Arm Community Blogs: Announcements (Nov. 16, 2021), https://community.arm.com/arm-community-blogs/b/announcements/posts/arm-cortex-x1c.

[34] Arm Ltd., Arm Neoverse E1 (2019), https://www.arm.com/-/media/global/products/processors/E1%20Solution%20Overview.pdf?rev=3834164b132c4cfba1ca29329b50833f&revision=3834164b-132c-4cfb-a1ca-29329b50833f.

[35] Arm Ltd., Cortex-A65AE, ArmDeveloper, https://developer.arm.com/Processors/Cortex-A65AE (last visited Feb. 27, 2024).

[36] Arm Ltd., Cortex-A65AE Automotive Enhanced, https://www.arm.com/-/media/global/products/processors/product_datasheet_cortex_a65ae.pdf (last visited Feb. 27, 2024).

3.   Many custom aspects of a processor are designed to match chip objectives

111.   In the past (e.g., 1970-1985), instruction set design was thought of as the primary job of computer architects. The challenges facing the computer architect beyond ISA design are particularly acute at the present, when the differences among instruction sets are small and when there are distinct application areas.

112.   Computer design entails identifying the required attributes, and then building within the constraints of cost while maximizing performance and optimizing energy. Irrespective of instruction set selection, the design process hinges on functional organization, logic design, and implementation, which is reflected in microarchitecture design, manufacturing technology and choices, and many other factors. This design process encompasses aspects like integrated circuit design, packaging, power, and cooling, and further requires a broad understanding of various technologies, ranging from compilers and operating systems to logic design and packaging.

113.   The ISA does not define the underlying hardware. As a result, a single architecture can be used for multiple use cases depending on the implementations. For example, Intel and Advanced Micro Devices (AMD) both sell various microprocessors belonging to the same x86 architecture. They all can run the same programs, but they use different underlying hardware and therefore offer trade-offs in performance, price, and power. Some microprocessors are optimized for high-performance servers, whereas others are optimized for long battery life in laptop computers. Often, many different microarchitectures exist for a single architecture. I describe some aspects of a microarchitecture in other sections of this report, and none of these microarchitectural

aspects can be derived from the ISA (rather the ISA only indicates the compatibility of the microarchitecture with programs).

4.   There are many similarities between ISAs

114.   The purpose of an ISA is to define a set of instructions needed to communicate operations to the hardware, like a vocabulary of commands that a computing hardware understands. While there may be differences in how individual instructions are structured, the basic functionality they describe are identical. For example, almost all architectures define basic instructions, such as add, subtract, and branch, that operate on memory or registers. This similarity may be expected because general-purpose computers may all need to perform such operations. Even when there are differences between the instructions available in different ISAs, such differences in instructions generally are not fundamental limitations of processor over another. For example, an instruction available in one ISA but not another ISA, but that instruction only defines functionality that can be implemented in the other ISA through a different instruction or a combination of multiple instructions.

115.   One of the primary drivers for similarity between ISAs is the commonality in foundational operation types that each ISA needs to support to aid the development of computer hardware. As described previously, computers perform operations based on machine instructions. These operations can be segmented into eight basic categories.

116.   I will note, ARM itself has acknowledged the minimal differences between architectures. In an interview, when asked "How do [] architectures differ from each other?" Richard Grisenthwaite, Executive Vice President and Chief Architect of ARM, responded

That's a really great question because it's easy to imagine that they will be radically different. . . . In reality, the nature of **what you can do on any particular architecture is really not that different**. . . . But in reality, the different architectures have quite a lot of **similarities in terms of functionalities they are able to offer. What makes an architecture successful is actually the number of people that use it**. You get this virtuous circle that as more people use your architecture, so - more people will want to use it and it becomes more popular. It's a self-fueling prophecy.[37]

5.   Arm ARM Overview

117.   In this section, I first briefly describe version 8 of the Arm Architecture Reference Manual or as referred to earlier, the Arm ARM, and its contents that describe the Arm architecture. For this section, I downloaded the Arm ARM from ARM's public website   at   https://documentation-service.arm.com/static/644a406baa78c007af74e6fd?token= (last visited February 21, 2024, also produced at ARM_00011869). I further explain that the Arm ARM only describes the architecture but does not provide an implementation of a microarchitecture. The Arm ARM includes architectural components that in order to implement as a processor require microarchitectural design, and as discussed further below, the Arm ARM does not describe microarchitectural elements.

i.   Aspects of the Arm ARM

118.   A microprocessor microarchitecture may be designed in such a manner as to be compatible with the software interface described in the Arm ISA, such as to perform certain operations when the microarchitecture receives a certain instruction from the Arm ISA compiled software application. In addition to the instructions, the ISA also describes the resources available to execute those instructions, such as registers, and a description of

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[37] Arm, *What is CPU Architecture?*, YouTube (Aug. 18, 2021), https://www.youtube.com/watch?v=KGHdDVLnKJM transcribed from audio.

how applications running on processors are expected to gain access to other key components such as memory resources. In the case of Arm, such architectural details are communicated to programmers and microarchitects through the Arm ARM. More specifically, the Arm ARM contains the following components:

- **Introduction to the Arm Architecture** – Part A of the Manual introduces the Arm architecture and describes the foundational concepts and designs associated with it, such as:

  o The Arm Architecture is a RISC (reduced instruction set computer) architecture with a large uniform register file and a load/store architecture with simple addressing modes. The Arm Architecture does not specify particular performance requirements or aspects and thus supports implementations across a wide range of performance points. ARM_00011869 at 11906.

  o The Arm Architecture is backward compatible, i.e., later versions of the architecture feature only additive changes over previous versions. For example, Section A2.9.1 describes the additional features added in v8.7 over previous versions. *Id*. at 11985.

  o The Arm Architecture features two execution states, or two different sizes of registers available to applications, called Aarch64 (64-bit registers) and Aarch32 (32-bit registers). *Id*. at 11906-11907.

- **Application Level Architecture** – Part B of the Arm ARM provides the details of the Arm Architecture required for application development. *Id*. at 12014. It describes the resources the Arm Architecture provides to any general application, i.e., an application

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that runs on a microprocessor but does not control the microprocessor itself. Examples

of resources that a microprocessor must make available include registers (both general

and special purpose) for use by instructions, and options available for an application

when instructions are executed in an unexpected manner. *Id*.

- **Instruction Set** – The Manual includes the Arm ISA and describes the types or classes

  of instructions, such as data processing instructions (e.g., arithmetic operations and load

  and store instructions to operate on memory), control instructions (e.g., branches that

  direct the overall flow of an application), and finally system instructions that can be

  used to signal other information to the microprocessor itself. *See, e.g., id.* at 12121. It

  also includes the encoding, i.e., the meaning of each binary bit in an instruction, and

  the order of the bits. Part C of the Arm ARM describes the instructions required for

  Aarch 64 while Part F describes those required for Aarch32. *Id*. at 12121; 19955.

- **System Level Programmer's Model** – While the Application Level Programmer's

  model describes how microprocessors compatible with the Arm Architecture function

  from the perspective of a general application, the System Level Programmer's Model

  describes resources available to developers of system software like Operating Systems

  that are capable of controlling the microprocessor and other general applications. The

  Arm ARM describes Exception Levels (EL) that an application must be allotted, which

  in turn determines the resources that must be made available. *Id*. at 12014.

  Furthermore, the System Level model also describes how an Arm Architecture-

  compatible microprocessor accesses the memory resources available to it and other

  features such as the debug and trace capabilities. Part D of the Arm ARM describes

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the system level architecture for AAarch 64, and Part G does the same for Aarch 32. *Id*. at 17213; 21605.

119.   Additional features of the Arm Architecture such as an external debug, i.e., a facility by which an Arm Architecture-compatible processor can be inspected by another external microprocessor unit when applications are improperly executing, and requirements for memory mapped components are included in Part H and I of the Arm ARM. *Id*. at 22937; 23429.

120.   The Arm ARM's purpose is to provide details of the Arm Architecture, and "is not intended to describe how to build an implementation of the PE [processing element]." *Id*. at 11905. The Arm ARM describes various components of the Arm Architecture but not how to build a specific microprocessor that is compatible with the Arm Architecture. ARM makes this very clear in its own documentation as it explains the difference between architecture and microarchitecture, stating that "Architecture does not tell you how a processor is built and works. The build and design of a processor is referred to as micro-architecture. Micro-architecture tells you how a processor works." Arm Ltd., *supra* note 5, at 12.

121.   In the excerpt reproduced below, ARM describes the information found in the Arm ARM, namely the Instruction set, Architectural registers, Memory model, and Exception model:

What information will I find in each document?

The following table shows which information is shown in the different types of documents:

-	Architecture	-	-	Micro-architecture	Micro-architecture	-
	Arm Architecture Reference Manual	GIC specifications	AMBA specifications	TRM	CIM	SoC Datasheet
Instruction set	x					
Instruction cycle timings				x		
Architectural registers	x	x				
Processor specific registers				x		
Memory model	x					
Exception model	x					
Support for optional features				x	x (some might be synthesis choice)	
Size of caches/TLBs				x		
Power management				x		
Bus ports				x	x	
All legal bus transactions			x			
Bus transactions generated by processor				x		
Memory map						x
Peripherals						x
Pin-out of SoC						x

Excerpt of Introducing the Arm Architecture[38]

122.   ARM describes what is included in each of categories when discussing its

meaning by architecture in the following excerpts:

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[38] *Id*. at 18.

3. What do we mean by architecture?

When we use the term architecture, we mean a functional specification. In the case of the Arm architecture, we mean a functional specification for a processor. An architecture specifies how a processor will behave, for example what instructions it has and what the instructions do.

You can think of an architecture as a contract between the hardware and the software. The architecture describes what functionality the software can rely on the hardware to provide. Some features are optional, as we explain in Architecture and micro-architecture.

The architecture specifies:

-	Description
Instruction set	The function of each instruction
	How that instruction is represented in memory (its encoding)
Register set	How many registers there are
	The size of the registers
	The function of the registers
	Their initial state
Exception model	The different levels of privilege
	The types of exceptions
	What happens on taking or returning from an exception
Memory model	How memory accesses are ordered
	How the caches behave, when and how software must perform explicit maintenance
Debug, trace, and profiling	How breakpoints are set and triggered
	What information can be captured by trace tools and in what format

Excerpt of Introducing the Arm Architecture[39]

123.   As shown in the prior excerpt above, ARM itself characterizes the Arm ARM as a functional specification that simply "describes what functionality the software can rely on the hardware to provide." *Id.* Notably, neither the software nor the hardware referred to here is Arm's but instead Qualcomm's and other software vendors. As further shown in the excerpt above, Arm acknowledges that the Arm ARM does not provide instruction cycle timings, processor specific registers, support for options features, size of caches/TLBs, power management, bus ports, and bus transactions generated by processor

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[39] *Id.* at 9.

that among many design choices when creating a microarchitecture.[40] The Arm ARM

further does not include a memory map, peripherals, or pin-out information for SoC

design.[41] Each of these must be designed by a microprocessor designer to perform these

operations in accordance with other design goals and trade-offs chosen by the designer.

ii.   Implementation Defined

124.   As described above, aspects of the Arm architecture specified the Arm

ARM include the instruction list, the memory and programming models. Per Arm, while

the architecture describes the rules associated with each of these components, it does not

describe the implementation of a specific microarchitecture. ARM_00011869 at 11905.

125.   This concept becomes strengthened by the fact that the Arm ARM declares

multiple aspects of architectural components as "Implementation Defined," which per the

Arm ARM, is behavior that is not part of the Arm Architecture but is defined by the

individual implementations, i.e., that designers are to make the appropriate design

decisions and build the appropriate hardware. *Id*. at 24792.   In fact, the term

"Implementation Defined" appears nearly 5000 times in the Arm ARM across the various

sections described in the previous section.

126.   Implementation defined architectural components exist across all aspects of

the Arm ARM that I described before. I will describe them through taking example from

the instruction set component itself.

127.   As described in the prior section, the Arm ARM lists instructions that can

be executed by a microprocessor, the functionality they are supposed to provide, and the

architectural registers, which are different than the actual physical registers in the processor

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[40] *Id*. at 18.
[41] *Id*.

that are available to the instructions. The implementation of the instruction (i.e., the HDL logic used to describe its functionality and the hardware that provides the functionality) is part of the microarchitecture and therefore not specified in the Arm ARM. In some cases, parts of an instruction's behavior are also declared as "implementation defined." For example, the Arm Architecture includes the CPYFP instruction (a Memory Copy Forward Only operation). This instruction is used to copy data between indicated memory locations. While the instruction would contain rules for the allowed memory locations (e.g., what types or portions of memory must be capable of being copied using the instruction), the exact amount of memory that can be copied with a single use of the instruction is implementation defined. Per the Arm ARM designers optimize the memory sizes based upon their requirements for the intended use cases. Such optimization is defined as part of the overall microarchitecture design.

128.   The table below provides a (<u>non-exhaustive</u>) list, and descriptions of implementation defined behavior that are left to the discretion of the microarchitect.

Category	Example	Source[42]
Exception Model	Prioritization of interrupts	D1-5383
Exception Model	Floating-point exception handling	D1-5372
Instruction Set	Size of memory blocked for exclusive access by Load-Exclusive Instruction	B2-225
Instruction Set	Behavior of Store-Exclusive instruction in relationship to Load-Exclusive Instruction	B2-226
Instruction Set	Encoding for Implementation Defined Instructions	C5-743
Instruction Set	Size of memory impacted with CPYFP and CPYFM instructions	C6-1366
ISA Independent Microarchitecture	Memory Hierarchy	B2-198

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[42] Page numbers refer to the Arm Architecture Reference Manual for A-Profile Architecture, Issue J.a., *supra* note 4.

Category	Example	Source[42]
ISA Independent Microarchitecture	Instruction Prefetching	B2-201
ISA Independent Microarchitecture	Cache Prefetching/Preloading	B2-202
Application-Level Programmers' Model	Size of memory region for memory-mapped peripherals	B2-183
System Level Programmers' Model	Powering of Core domains and Debug domains	D1-5392
System Level Programmers' Model	Behavior of caches during resets	D1-5393
Application-Level Programmers' Model	Maximum length of Floating-Point Control and Floating Point Status Registers (FPCR, FPSR)	B1-148
Application-Level Programmers' Model	Behavior of SSBS register during warm reset	C5-842

Examples of Implementation Defined behavior in the Arm architecture

B. **The ▮▮▮▮▮▮▮ Design Reflects Significant Engineering Effort**

129.   The ▮▮▮▮▮▮ Design, like all of Qualcomm's Product Designs, demonstrate originality and creativity in microarchitecture that are not derived from the Arm ARM. As discussed in the previous section, the Arm ARM does not provide details on how to build a microarchitecture including an SoC design. Qualcomm's originality and creativity is expressed in two primary manners: its design choices and the implementation of those design choices.

1. **Originality and Creativity in Microarchitecture**

130.   In this section I discuss some microarchitectural features that differentiate various implementations of the same architecture. Even with small changes to their size or implementation, design decisions can potentially have significant performance

consequences resulting in very different microprocessors (although those different microprocessors may all be compatible with the Arm ISA).

i.   Cache Organization, Access, & Performance

131.   To execute instructions, the datapath portion of the processor accesses pieces of memory, potentially both outside and within the microprocessor.   The organization and implementation of memory access involves many trade-offs for the microarchitecture design and performance.

132.   There exists a hierarchy of memory that the processor accesses: registers, caches, memory, and storage. Caches and registers are within the processor, while memory and storage are outside the processor. Organization and access to registers and caches are differentiating factors for microarchitecture because the faster the processer can access data, the faster it can execute instructions on that data. Register files, being small and fast, are preferred for storing frequently used variables, while memory, which is larger and slower, is used for less frequently accessed data. In the context of the ARM architecture, all operations are performed directly on registers. Therefore, any data that is initially stored in memory needs to be transferred to a register before any processing can occur. A designer designs where data is stored and how the data is transferred in and out of registers to other memory.

133.   In general, the smaller the memory, the faster is its speed, and the faster the memory, the more expensive the memory (in terms of dollars) which holds true across all applications. Memory hierarchy is organized differently according to different market specifications.

134.   One of the aims of a competitive microarchitecture is to speed up the access and retrieval of cache. For example, one technique to reduce the time a microprocessor takes to find a data item in a cache (also called cache "hit" time) is way prediction. Using a way prediction technique, extra bits are kept in the cache to predict the way (or the block within the set) of the next cache access. A designer's implementation of prediction and the design choices the process entails are not specified by the ISA.

135.   Another improvement on cache access is decreasing the proportion of references to a level of the memory hierarchy (e.g., cache) in which the requested data is not found in the requested level, and therefore needs to be fetched from elsewhere. This is referred to as a "miss rate." One technique to reduce cache miss rate is called hardware prefetching. As the name implies, this technique prefetches items before the processor requests them. Data and instructions can be prefetched into caches or an external buffer, both are quicker to access than main memory. For example, a microprocessor can fetch two blocks on a miss (1) the requested block and (2) the next consecutive block. Here the requested block is placed into the instruction cache, and the prefetched block is placed into the instruction stream buffer. The original cache request is canceled if the requested block is in the instruction stream buffer. Like way prediction, hardware prefetching and its design are not specified by an ISA.

136.   The access to cache and the speed or accuracy of it are not the only differentiating attributes of a microarchitecture implementation related to caches. Microarchitecture corresponding to the cache hierarchy also requires, for example, policies and algorithms for storing data in the cache or removing it, e.g., spatial or temporal caching, all of which impact the performance of a microprocessor and are not specified by the ISA.

ii.   Parallelism

137.   As the name implies, parallelism involves performing tasks in parallel instead of sequentially. In a microarchitecture, parallelism is a technique that improves the speed and hence the throughput of instruction execution. Implementation of parallelism comes in two forms – spatial and temporal. Spatial parallelism involves the use multiple copies of hardware so that multiple tasks can be done at the same time, and using temporal parallelism a task is broken into stages, like an assembly line. Spatial parallelism is part of a microprocessor design in "multicore processors," and temporal parallelism is part of microprocessor designs in "pipelining." Both concepts are described further below.

iii.   Pipelining

138.   The figure reproduced below shows how pipelining allows for more instructions to be executed in the same amount of time when compared to a non-pipelined processor (i.e., single-cycle processor) for a simple 5-stage pipeline. Pipelining is not simple, and its implementation introduces complexity and impacts power and performance.

139.   Even with the improvements made, pipelining introduces complexities called hazards (structural, data, and control); control hazards occur when executing instructions related to branching. To address these hazards, a technique referred to as branch prediction is used that assumes the outcome for a conditional branch opposed to waiting for an actual outcome. However, branch prediction introduces the possibility of misprediction, which also affects performance.

140.   While these techniques affect performance, neither the pipelining nor the staging or branch prediction design of a microarchitecture is defined by the ISA.

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iv.   Multicore Processors

141.   In addition to implementing instruction-level parallelism techniques, data-level parallelism can be leveraged for further performance improvements.   A multiprocessor system consists of multiple processors or cores and a method for communication between the processors. Multiple cores in a microprocessor can improve performance, but it also increases overall complexity and requires additional design considerations.

142.   Memory organization and access for multiple processors is one design decision a designer makes when implementing a multicore design.   There are many multicore design choices available, including centralized shared memory design and distributed shared memory design. This decision depends on how the multicore processors are designed to act harmoniously, and each option has its own complexities during implementation. Similar to pipelining, an ISA does not describe the microarchitecture design and implementation of a multicore processor.

143.   As discussed previously, as acknowledged by Arm's own documentation, the Arm ARM does not provide a microarchitecture.

2.   ▮▮▮▮ Microarchitecture Design

144.   In this section, I will discuss microarchitecture designs found in the ▮▮▮▮ SoC and the ▮▮▮▮▮▮ Design. As I show below, the ▮▮▮ SoC including the ▮▮▮ ▮▮▮▮ Design exemplify the originality and creativity of microarchitecture design. ▮▮▮

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      i.   █████ **SoC**

145.   The █████ SoC, which was designed by Nuvia and Qualcomm independently from any ARM Technology under their respective ALAs, contained Qualcomm's custom-designed ███████████ Design. The ███████████ Design was designed to be compatible with the Armv8.7 architecture. Neither Dr. Colwell nor Dr. Chen provide analysis of the ██████ SoC codebase or microarchitectural design, which is not surprising given that the Arm ARM does not provide an SoC design.

146.   SoCs encapsulate entire systems integrated onto a single die or multiple dies, where the CPU is one component. SoCs may include memory controllers, I/O interfaces, hardware accelerators, etc., all based on target application areas. *See* QCARM_0356885. SoC design requires detailed understanding of packaging, I/O pin behaviors and none of these aspects are part of any ARM Technology. The Arm ARM does not contain any information related to the development of an SoC, as Mr. Grisenthwaite acknowledged at his deposition, and further for the reasons I describe above about what the Arm ARM contains. *See* Grisenthwaite Tr. at 220:10–13 ("Q The ARM ARM does not provide information on how to make an SOC, does it? A No.").

147.   The ██████ SoC incorporates Nuvia's ███████████ Design innovations, and Qualcomm's ███████████ Core innovations, along with other SoC layer innovations, ██ ███████████ *See* QCARM_0356885 at 96. The ██████ SoC design targeted server systems. *See id*. at 890.

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      ii.   ███████████ **Design**

163.   In this section, I will provide a brief overview of the ███████████ Design's microarchitecture (as existing at the time of acquisition), highlighting its

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3.   **Nuvia Received no Assistance from Arm with the Development of the Microarchitecture of the** ███████████ **Design**

207.   It is unlikely that Arm could provide ███████████ SoC engineers assistance in the microarchitecture implementation of the ███████████ Design. ███████

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██ ARM engineers, including Mr. Grisenthwaite may be familiar with Arm ARM, but not the ███████ ███████ Design microarchitecture intricacies. Arm never saw the RTL for the ███████ ███████ Design or for any of Qualcomm's Cores, which Mr. Grisenthwaite acknowledges would contain Nuvia or Qualcomm's "proprietary knowhow [or] secret source." *See* Grisenthwaite Tr. at 76:10–77:2. Dr. Colwell refers to weekly meetings that discussed Architecture Compliance Kit ("ACK"). *See* Colwell Report ¶ 140. ███████████████

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C.   The ACK Does Not Provide Information for ████████ a Microprocessor Nor Is It ██████████ in a Microprocessor

208.   Dr. Colwell contends that the "ARMv8-A Architecture Compliance Kit," is included in ██████████████. ARM_00057230 at 231. The ACK for short is a set of tests that are used to determine compliance of a microprocessor design with the Arm ISA. That is, the ACK determines whether the microprocessor is compatible with the Arm ISA. These tests produce nothing other than output values that can be compared to an "answer key" to determine if the microprocessor produced the expected result that an Arm ISA-compatible microprocessor would produce. This allows Arm to verify that different microprocessor designs from different Arm licensees produce consistent results, and allows application developers to be confident that their applications will work across different microprocessors. The ACK tests do not create or modify the microarchitecture RTL or product designs, nor do they provide instructions to a microarchitect as to how to fix any identified failures. *See*, Agrawal Tr. at 34:8–17; Grisenthwaite Tr. at 92:8–10.

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209.   I understand that Qualcomm's position is that the ACK is not ██████ ██████████ under the Nuvia ALA based on interpretation of the definition of Annex 1 of the Nuvia ALA and testimony from Mr. Grisenthwaite. Nevertheless, even if the ACK is considered ██████████████, I do not believe that any of the Qualcomm Cores or products were ██████████████████████

210.   Neither the tests themselves nor the outputs of the tests provide information from which a designer can design a microprocessor. Dr. Colwell opines that "an ARM licensee would . . . not[e] which tests passed and which did not, as a way of focusing the development team on the parts of the design that were not yet implemented correctly."

Colwell Report ¶ 81. This assertion is not correct. Microarchitecture designers and circuit designers have to create their own unit level tests to test the microarchitecture implementation's correctness. These unit level tests have a huge complexity that far outweighs the complexity of the Arm ACK as I describe in the next paragraph. The ACK can only point to an issue that does not demonstrate compatibility with the Arm ISA. However, there is no content in the ACK's report analysis to instruct the designer to make a certain change in the microarchitecture. At most, the output is a flag to look at a particular portion of the microarchitecture. This should be expected because, as I describe above, a microarchitecture is a very custom and unique aspect of a microprocessor that reflects the creativity and decisions of the designer. Given the infinite number of potential microarchitectures that can be Arm ISA-compatible, generic tests such as those in the Arm ACK could never provide useful information to a designer for how to revise or fix any aspect of the microarchitecture design that may have failed a test for their particular microarchitecture design. ███████████████████████████

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211.   The test suites that Arm provides cannot test the microarchitecture innovations in Qualcomm's Cores because it is not possible to provide test suites for features that Arm does not even know exist in a given processor. For instance, Arm test suites do not know the presence of features such as branch order buffers, caches with specific configurations. The Arm test suites only provide instruction functional testing. For instance the test suites may run an Arm ADD instruction with two known inputs and compare the computed output with the known value. But such a test cannot determine the speed or the power consumption of such an operation in Qualcomm's own processors.

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ARM support does not resolve the microarchitectural bugs that may arise in Qualcomm's implementations. The support team does not provide microarchitecture.

212.   Dr. Colwell claims that the compliance kit (ACK) "is used to help establish whether a given CPU is Arm-compliant. It is basically a comprehensive set of tests, created and developed over several decades, where each test is aimed at some aspect of the Arm ISA to verify it has been implemented in an architecturally acceptable way." Colwell Report ¶ 81. But, as I described above, the ACK only does "architectural" testing, not the microarchitectural testing. ███████████████████████████

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D.   ARM Crypto Does Not Provide Information from Which to ████████ or Which Is ███████████ in, a Microprocessor

214.   I also disagree with Dr. Colwell's statement that "if a licensee has chosen to implement the crypto extensions of the Armv8, obviously the instruction decoder design will necessarily reflect that, since it has to detect and decode all CPU instructions." Colwell

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Report ¶ 87. I understand that Qualcomm's position is that the Crypto extensions are not ███████████████ under the Nuvia ALA based on interpretation of the definition of Annex 1 of the Nuvia ALA and testimony from Mr. Grisenthwaite. Nevertheless, even if the Crypto extensions are considered ██████████████, I do not believe that any of the Qualcomm Cores or products were █████████████ the Crypto extensions for the same reasons that aspects of the Arm ARM were not █████████████████ for the reasons described above.

215.   Even if some of the Crypto instructions are decoded in a decoder, ████████

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██████ Additionally, the security instructions such as SHA-1, SHA256, and AES are standard cryptographic primitive () and multiple ISAs support SHA implementations.

E.   No Core Was an ██████████████████████ Under the Nuvia ALA

216.   Dr. Colwell concludes that ████████████████████████

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██████████████ Colwell Report ¶ 145. I disagree ████████████████████

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F.   **Qualcomm's   Product   Designs   are   Not   a** ████████   ████████
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VII.   QUALCOMM'S CODEBASES DO NOT SUPPORT DR. COLWELL'S OR DR. CHEN'S OPINIONS

253.   Dr. Colwell opines that "the March 14, 2021, Nuvia ██████ code is ████

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████████████████ and "Nuvia and Qualcomm designs after the March 14, 2021,

Nuvia ██████ code are also ████████████████████████████

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██████████████ *Id*. ¶166. Surprisingly, Dr. Colwell attempts to support his opinions using

the high-level comparison analysis of different codes bases, none of which were written by

Arm, as performed by Dr. Chen and his single day of review of the Qualcomm Codebases

produced in this case.   *Id*. ¶¶156-167.   Dr. Colwell "endorse[s] the qualitative and

quantitative conclusions from Dr. Chen's expert report, namely that: ████████████

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[46] While this portion of Dr. Colwell's summary of Dr. Chen's conclusions is not entirely clear, Dr. Chen does not conclude that "██

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█████████████████," and instead he states it is his "opinion that the March 14, 2021

████████ RTL code ████████████████████████████████████

████████████████████████████" Chen Report ¶ 19.

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██ *Id.* ¶ 162.

I disagree with Dr. Colwell's opinions and Dr. Chen's qualitative and quantitative conclusions.

254.   First,   Dr.   Chen's   quantitative   conclusions—██████ ████████

██—even if true, does not demonstrate that Qualcomm's Product Designs after March 14, 2021 are

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████████████████   This RTL code was developed independently by Nuvia, and Dr. Chen, under his quantitative analysis, has not shown otherwise.[47]

255.   Second, neither Dr. Colwell nor Dr. Chen has shown that "the March 14, 2021, Nuvia ████████ code" is ████████████████████████████████

████████████—nor can they. Dr. Chen states he identified "features/instructions that appear to be specific to Arm" in the "March 14, 2021 ████████ code" that are ████████████

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████   Chen Report ¶¶ 36-51. To be clear, what Dr. Chen identifies in the March 14, 2021 ████ code is RTL created by Nuvia that is ████████████████████████

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[47] I have been informed by counsel that ████████████████████████████████ ████████████   Dr. Colwell and Dr. Chen did not offer any opinions regarding Qualcomm's development efforts under its ALA. If Dr. Colwell or Dr. Chen are permitted to do so in the future, I reserve the right to respond.

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256.   I have been informed that the termination obligations in ██████████ of the

Nuvia ALA only concern the ██

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██████████   QCARM_0337839 at 852.   Accordingly, my understanding is that the

comparison of the various Qualcomm Cores is an inappropriate examination, as the

appropriate test is to determine whether the Qualcomm Cores are ████████████████████

████████████   Nevertheless, I have examined Dr. Chen's analysis and Dr. Colwell's reliance

on Dr. Chen's findings.

257.   Moreover, as I will further explain below, Dr. Chen's analysis and

conclusions are fundamentally flawed and do not support Dr. Colwell's opinions.

A. Dr. Chen's quantitative comparisons are unreliable

258.   For his quantitative analysis, Dr. Chen compared "March 14, 2021, Nuvia

██████ code" (as a baseline) to other Qualcomm Codebases for ████████████████████

████████████████████.   Chen Report ¶¶ 22-26.   Dr. Chen describes that he performed

his quantitative analysis in two ways by: "(1) identifying key folders and comparing files

within those folders across different SOC/core versions, and (2) identifying top-level RTL

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files of key building blocks and comparing each of the RTL files across different SOC/core

versions." *Id*. ¶ 26.

259.   Based on his quantitative analysis, Dr. Chen concludes that ▮▮▮▮▮▮▮▮

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▮▮▮▮▮▮▮▮   *Id*. ¶ 18. However, in my opinion, as explained further below, Dr. Chen's

quantitative analysis is unreliable because he ignored a majority of Qualcomm's

Codebases, omitted critical folders and files, and chose too large of a skew tolerance when

he compared Qualcomm's Codebases.

1.   Dr. Chen's comparisons omit a majority of Qualcomm's Codebases, including critical folders and files

260.   As a preliminary matter, I will note that Dr. Chen's quantitative analysis

ignores a majority of the Qualcomm Codebases for Qualcomm's Product Designs yet also

fails to constrain his analysis to code that is allegedly ▮▮▮▮▮▮▮▮▮▮▮▮▮▮

▮▮▮▮▮▮▮▮   Dr. Chen's quantitative analysis utilizes only a subset of ▮▮▮▮ folders

and ten files within these folders from the Qualcomm Codebases. *Id*. ¶¶ 28, 33. As further

discussed below, by selecting a limited set of folders and files, and further ignoring portions

of Qualcomm's Codebases that are critical, Dr. Chen's analysis is unreliable

i.   Folders Excluded from Analysis

261.   Dr. Chen's quantitative analysis includes only 14 top level RTL folders

from a single directory, ▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮. Dr. Chen's quantitative analysis

excludes ▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮▮

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██ It is my

opinion that these excluded folders contain source code that is necessary for developing,

building, and testing the CPU Core and the associated SoC designs. The figure below is

illustrative of the structure of Qualcomm Codebase.
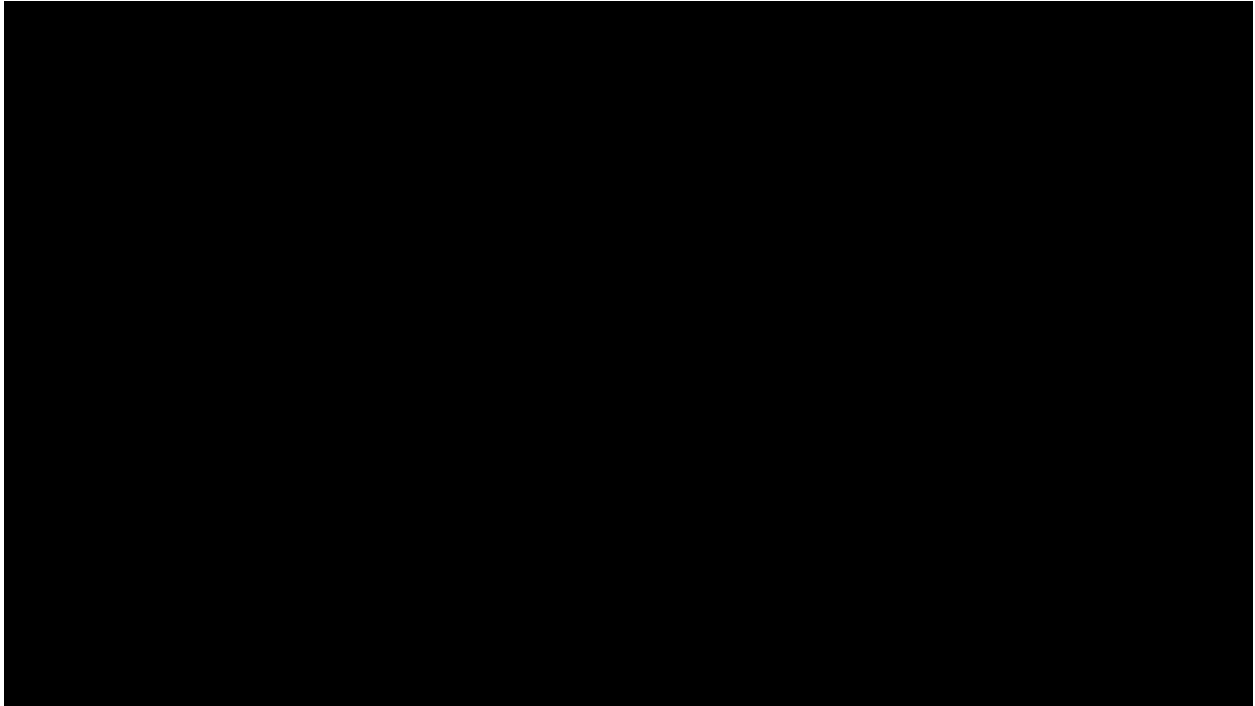
Illustration of Directory Structure for Qualcomm Codebase

262.   First, by excluding all folders other than ███, Dr. Chen's analysis misses

several files and folders that implement key functionality of various Qualcomm Product

Designs. SoC code is extremely important as it contains various components required for

correct functioning that are developed and contained outside the ███ source code. As an

example, █████████████████████████████████████

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██████████████████████████████████████ Another

example of an important SoC source code component is that of ████████████████

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████████   Dr. Chen excludes this important ███████████   code in his quantitative

analysis. The SoC source code also contains important RTL code that defines and controls

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263.   Second, within the ███ directory, Dr. Chen narrows his analysis to only the

█████ folder. But the source code present in folders outside the ███████   directory are

necessary for the development of Qualcomm's Cores. For example, Dr. Chen points out

that in his quantitative analysis he excludes the ██████████████████████████

█████ *Id*. ¶ 29. This folder resides within the source code snapshots corresponding to all

versions of Qualcomm's Cores. The files within this folder contain ██████████████

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264.   Another folder Dr. Chen excludes is the ████████ folder. Files in this folder

play a crucial role in the development process as ██████████████████████████

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██   By choosing

to ignore such files, Dr. Chen is presenting a less than comprehensive analysis and does

not contextualize the complexities of developing a functional CPU Core.

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265.   Even within the single ███████ directory, Dr. Chen's analysis excludes several key folders that are crucial to the CPU Core. For example, Dr. Chen includes 10 top level RTL folders (and 4 library folders) from a single directory, ████████, related to the ███ (*Id*. at Table 1). This directory exists in all the code base snapshots and has different total number of folders in each. As Table 1 suggests these folders constitute only a small portion of the ███████ folders, which itself is one among various other folders within the ███ directory[49].

ID	Source Code Snapshot	Total top-level folders in ███████ directory	% of folders in ███████ excluded by Dr. Chen
1	███████ 3/14/2021	██	██
2	10/24/2023	██	██
3	7/28/2023	██	██
4	███████ 7/28/2023	██	██
5	███████ 7/28/2023	█	██

Folders excluded by Dr. Chen in ███████ directory

266.   Dr. Chen further restricts his analysis to certain folders within the ███████ directory to 14 folders. Dr. Chen's explains that he "did not consider ███ ██ ███████████████████████████████████ *Id*. ¶ 29. Dr. Chen's restriction here is incorrect. For example, Dr. Chen's analysis does not include the ███████ ██████████████████████████████████, a component that provides crucial functionality for Qualcomm's Cores and most microarchitectures generally. Similarly, he has ignored the ██

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[49] Table presents relevant data for snapshots containing the most up to date source code corresponding to the CPU Core in a given SoC i.e., ███████ dated 10/24/23, ███████ dated 7/28/23, ███████ dated 7/28/23, and ███ dated 7/28/23.

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267.   Dr. Chen's quantitative analysis further misses a crucial segment of the codebases associated with the ███████████████████████ – the folders and files associated with the ██████████████████████████

i.   **Files Excluded from Analysis**

268.   In the second part of his quantitative analysis, Dr. Chen selects ten top level RTL code files within ███████████████ folders (the same folders discussed previously) to compare across Qualcomm's Codebases. *Id.* ¶ 33. Dr. Chen asserts that "[t]hese files are important because they are the top-level RTL code files in the important design hierarchies and key functional CPU blocks listed in Table 1." *Id.* As a preliminary matter,

by ignoring all the other files in a folder, Dr. Chen's quantitative analysis misses important features and unique implementations of each individual CPU block. Typically, the top-level file for a CPU module lists the constituent submodules and how they are connected to each other. However the functional details of the CPU block are usually described in the submodule files rather than the top level file. For example, ███████████████

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████████████ By including only the top-level files, Dr. Chen's analysis excludes key microarchitectural implementation differences between two snapshots.

2. Dr. Chen's quantitative comparisons are meaningless

269. Not only did Dr. Chen's quantitative analysis omit a majority of Qualcomm's Codebases including crucial folders and files, but the comparison criteria used does not yield reliable outcomes. For his quantitative analysis to compare the folders and files above, Dr. Chen used a tool named Beyond Compare. Chen Report ¶ 27. Dr. Chen presents two values for the folders and files above, "File name similarity" and "Line similarity." These are presented in Tables 2 – 6 and 8 – 12 of the Chen Report. I found that the "Line Similarity" values vary significantly based on (1) the choice of folders and files and (2) the choice of Skew Tolerance value in Beyond Compare, the tool used for comparison.

270. According to Dr. Chen, the "File name similarity" values reflect the percentage of files in a folder that have identical names to files in the folder of the same

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name in the baseline version of the code while "Line Similarity" values reflect the percentage of identical lines between two versions of a folder or file of the same name. As a preliminary matter, two file names could be identical but their content could be different. Two directory structures may be similar but their directory contents could be different. To calculate the "Line Similarity" metric, Dr. Chen uses the Beyond Compare tool and describes that he (1) generates a statistical report using the "folder comparison" function of Beyond Compare, and (2) calculates the "Important line similarity" between two files which he describes as the result of dividing the "Number of identical important lines" with the total number of "Original important lines".

271.   Beyond Compare assesses the lines of code similarity between two versions of code files by selecting each line of code in one file (say an earlier version) and assessing its existence in another file (later version). One of the important configurations in Beyond Compare is called the "skew tolerance." The skew tolerance defines the number of lines within the later version of file that the software will use to look for the purported line of code from the older version. For example, a skew tolerance (ST) of 2000, a default value in the software, implies that a given line from the older version is compared with all the lines of code that are 2000 lines ahead of and after it in the newer version. Dr. Chen uses 2000 as the skew tolerance while calculating the "Line similarity" values. *Id*. ¶ 27.

272.   While his report does not sufficiently describe his method for calculating identical important lines, through his notes (QCARM_7517717 (shared separately as part of his report)), I was able to assess his method. It is my understanding that Dr. Chen uses a snapshot of ██████████████████████████████████████ core as the "Original" in Beyond Compare. Additionally, the "identical important lines" are

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calculated for the entire folder although Dr. Chen describes it as for individual files in his report. Chen Report ¶ 32 .

273.   As described earlier, Dr. Chen's quantitative analysis is restricted to only a specific set of folders within ███████, and he also highlights the similarity values of specific files that he deems important. I have expanded Dr. Chen's analysis to include additional folders within ███████ that he has excluded. Additionally, in source code corresponding to ██████████████████████████████ Cores he excludes the folders related to the ██████████████████████████, which I have included in my analysis. I have also expanded my analysis to include top level RTL files from the folders that he has excluded.

274.   I present my results in the table below. To produce these, I have followed the steps described by Dr. Chen in Paragraph 32 of his report and based on his working papers when the description in the report was insufficient. As evident from these tables, the average similarity values for the folders and files Dr. Chen excluded ████████ ██████████████████ (calculated as the average of the values presented in Tables 3 – 6, and 9 – 12 of the Chen Report). ████████████████████████ ████████████████████████████

Line similarity values for folders excluded by Dr. Chen at a Skew Tolerance value of 2000

Average line similarity values for folders included and excluded by Dr. Chen,
and overall average at a Skew Tolerance value of 2000

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Line similarity values for files excluded by Dr. Chen at a Skew Tolerance value of 2000

Average line similarity values for files included and excluded by Dr. Chen, and overall average at a Skew Tolerance value of 2000

275.   Dr. Chen's results, in addition to being dependent on the choice of folders and files, also vary based on the Skew Tolerance (ST) setting of Beyond Compare. As described earlier, Dr. Chen uses the Beyond Compare tool to perform his quantitative analysis. Within Beyond Compare, he sets the ST value to the default value of 2000. The effect of the ST setting on Dr. Chen's results is illustrated in the tables below. To produce

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these tables, I have followed the steps described by Dr. Chen on folders and files chosen by him with the only difference being that I used two different Skew Tolerance (ST) values. First, I selected a value of 100 for the Skew Tolerance setting (ST100). Then I used the "Unaligned" setting which is the equivalent of a Skew Tolerance value of 0 (ST0) i.e., it directs Beyond Compare to count two lines as identical only when they are in the exact same position across both versions of a file. Therefore, only files that have a 100% similarity under ST0 settings are identical copies.

276.   As evident from the tables, the line similarity values at ST 100 and ST0 are lower than those at ST2000, both at folder and file level calculations, and in particular no file or folder in any snapshot is an identical copy of a file or folder of the same name in the baseline version. It is also evident that the ST parameter is an important variable that affects the output similarity values. Dr. Chen provides no support whatsoever for using 2000 as the Skew Tolerance value. Chen Report ¶ 27.

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██████ – **Line Similarity Percentages when compared to 3/14/21** ████ **(baseline) (ST 2000 values from Table 3 of the Chen Report)**

██████ – **Line Similarity Percentages when compared to 3/14/21** ████ **(baseline) (ST 2000 values from Table 4 of the Chen Report)**

████████ – **Line Similarity Percentages when compared to 3/14/21** ████ **(baseline) (ST 2000 values from Table 5 of the Chen Report)**

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■■■ – Line Similarity Percentages when compared to 3/14/21 ■■ (baseline) (ST 2000 values from Table 6 of the Chen Report)

■■■ – Line Similarity Percentages when compared to 3/14/21 ■■ (baseline) (ST 2000 values from Table 8 of the Chen Report)

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██ – Line Similarity Percentage when compared to 3/14/21 ██ (baseline) (ST 2000 values from Table 9 of Chen report)

████ – Line Similarity Percentage when compared to 3/14/21 ██ (baseline) (ST 2000 values from Table 10 of Chen report)

██ – Line Similarity Percentage when compared to 3/14/21 ██ (baseline) (ST 2000 values from Table 11 of Chen report)

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277.   Given the total number of lines of codes present in each folder, the ST 2000 value used by Dr. Chen is simply an inaccurate parameter. To demonstrate this I calculated the mean and median values for the total number of lines in the folders and files used by Dr. Chen. The table below shows the results. As is evident from the tables, the ST 2000 value used by Dr. Chen comes nowhere closer to any values in the table. Thus, if a line of code appears anywhere in the entirety of the other file that is being compared, Dr. Chen considers such a line to be similar for his analysis. Considering that the choice of ST has such an outsized effect on Dr. Chen's results and given the lack of proper support for an ST value of 2000, Dr. Chen's analysis cannot reasonably support his conclusions.

Median of number of lines of code per file in folders across source code snapshots

Mean of number of lines of code per file in folders across source code snapshots

279.   Analysis using different criteria that I present above demonstrates █████

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The comparisons are attached as Appendix B. One excerpt from Appendix B is reproduced below as an example from those comparisons. This excerpt shows the two files being compared as Left and Right file as seen in the title of the excerpt below. The Left file line numbers and Right file line numbers are shown in the first and second columns of this excerpt.

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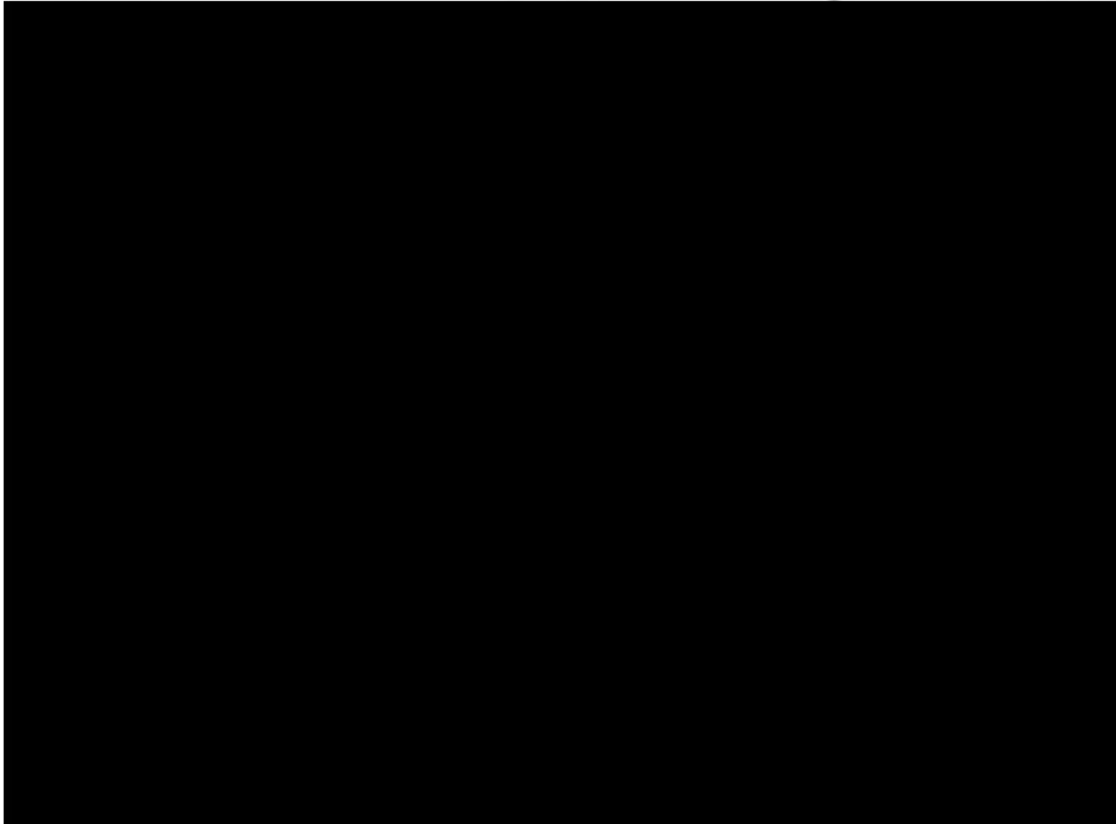
Excerpt from a diff compare of ███████ **between** ███ **and** █████ **Codebases**

QSC2ARMVQC0000102.

280.   If the lines in the Left and Right file are identical, then the excerpt shows the two matching lines. For example, the matching of the curly brace "}" is reported as a matching line in the above excerpt as line 53 in the left file and line 340 in the right file. Clearly, a curly brace match says nothing about the code in this example. When two lines differ, they separate and are shown individually. As seen in the excerpt above, this comparison between ████████ Design Codebase (March 14, 2021 ████ code) and the ████ Core Codebase illustrates the drastic differences between Qualcomm's Codebases.

281.   Taken together, Dr. Chen's quantitative analysis is unreliable because he ignored a majority of Qualcomm's Codebases, omitted critical folders and files, and chose

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too large of a skew tolerance when he compared Qualcomm's Codebases. For example,

when view with proper criteria, when compared, Qualcomm's Codebases have a low level

of similarity. ██

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B.   **Dr. Chen's qualitative analysis does not demonstrate any of the Qualcomm Codebases are** ████████████████████

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ARM_00011869 at 18631.

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C. **Qualcomm's Cores and Qualcomm's Product Designs do not ██████████ the ████████████ Design**

304.   Dr. Colwell opines that Qualcomm's documents show that Qualcomm

incorporated ██████████████████████████████████████

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██████████████████████ Colwell Report ¶ 113. I disagree. The Qualcomm documents

cited by Dr. Colwell do not provide sufficient support to conclude that Qualcomm ████

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████████   *Id.*   ¶¶110-113   ████   ████████████████   ████████████

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305.   The   necessity   to   develop   market-specific   applications   for   a
microprocessor's commercial success cannot be overstated. Qualcomm has undertaken the
challenge of designing and developing market-specific applications for distinct domains

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These sectors, each with their unique requirements and constraints, demand tailored design
approaches that are fundamentally independent of the underlying architecture.   For
instance, server applications prioritize performance and scalability, mobile applications
focus on energy efficiency and compactness, compute-intensive applications demand high
computational power and efficiency, and automotive applications require robustness and
safety   compliance.   This   segregation   leads   to   significant   design   choices   in
microarchitecture, influencing aspects such as power consumption, processing speed,
physical size, and heat dissipation, ultimately shaping the technology to meet the specific
needs and challenges of each market segment.

306.   As   an   example,   in   this   section,   I   will   discuss   certain   significant
microarchitectural differences between Qualcomm's Product Designs for the ██████
██████ Design and the ████████████ Core, which reflect a strategic shift from the ██████

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[56] ████████████████████████████████████

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to ███ markets. For this section, my summary reflects my review of ███

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314. The following table gives representative examples of each type of change described above.

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315.   In addition to the significant differences necessitated by market-specific needs, Dr. Colwell and Dr. Chen do not analyze the architectural differences in the ████████ Core, which ███

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VIII.   QUALCOMM'S PRODUCT DESIGNS WERE IMPACTED BY THE SWAP OUT

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A. ██ **Were Involved in the Swap Out**

320.   Dr. Colwell relies on Dr. Chen's report, in which Dr. Chen compared "the February 28, 2022 ████ code with the April 1, 2022 ████ code to determine the differences between these two versions of code." Chen Report ¶35. For this comparison, Dr. Chen used the same 14 high-level RTL folders and 10 files discussed previously from the ████████ folder. Chen Report ¶35. Dr. Chen concludes that these ████████████ ██ *Id*.

321.   ██

██████████████████████████████ As explained in my Opening Report, all Nuvia-sourced ARM RTL was swapped out for identical Qualcomm-sourced ARM RTL. *See* Opening Report ¶¶ 73-124. ████████████████████████████

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IX.   RESERVATION OF RIGHTS

322.   My opinions are subject to change based on additional opinions that ARM's experts may present and information I may receive in the future or additional work I may perform. With this in mind, based on the analysis I have conducted and for the reasons set forth above, I have reached the conclusions and opinions in this report.

323.   At trial and as discussed above, I may rely on visual aids and may rely on analogies concerning any related technologies.

324.   In connection with my anticipated testimony in this action, I may use as exhibits various documents produced in this case that refer or relate to the matters discussed in this report I have not yet selected the particular exhibits that might be used. In addition, I may create or assist in the creation of certain demonstrative evidence to assist me in testifying, and I reserve the right to do so.

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I certify under penalty of perjury that the foregoing is true and correct.

Date: February 27, 2024

Murali Annavaram, Ph.D.

Los Angeles, California

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

ARM LTD.,	
Plaintiff,	
v.	C.A. No. 22-1146 (MN)
QUALCOMM INC., QUALCOMM TECHNOLOGIES, INC. and NUVIA, INC.,	
Defendants	

REBUTTAL EXPERT REPORT OF DR. MURALI ANNAVARAM

APPENDIX A
Materials Considered

EXHIBIT A

MATERIALS CONSIDERED

1. **Documents referenced in my Rebuttal Expert Report.**

2. **Docket (Arm Ltd. v. Qualcomm Inc. et al., No. 1-22-cv-001146 MN (D. Del.)):**

D.I. 1, Complaint, dated August 31, 2022

3. **Discovery Responses, witness deposition transcripts, and exhibits thereto, including:**

2023.10.12 – Gulati, Manu Deposition Transcript
2023.10.27.23 – Sharma, Nitin Deposition Transcript
2023.11.03 – Williams III, Gerard Deposition Transcript
2023.11.08 – Ashgar, Ziad Deposition Transcript
2023.11.17 – ARM's Second Supplemental Objections & Responses to Qualcomm's First Set of Interrogatories
2023.11.17 – Qualcomm's Supplemental Responses & Objections to ARM's 1st Set of ROGs (Nos. 7-12)
2023.11.29 – Bos, Lynn Deposition Transcript
2023.12.19 – Tran, Christine Deposition Transcript
2023.11.15 – Grisenthwaite, Richard Deposition Transcript
2023.10.25 – Trivedi, Jignesh Deposition Transcript
2023.12.14 – Agrawal, Vivek Deposition Transcript
2023.12.12 – Haas, Rene Deposition Transcript
2023.12.20 – Opening Expert Report of Dr. Robert Colwell ("Dr. Colwell Report")
2023.12.20 – Opening Expert Report of Mike Chen ("Dr. Chen Report")

4. **Produced Documents**

ARM_00000848
ARM_00003097
ARM_00004675
ARM_00011869
ARM_00032734

Exhibit A to Rebuttal Expert Report of Dr. Murali Annavaram

ARM_00037427
ARM_00057230
ARM_00063625
ARM_00067433
ARM_00068711
ARM_00099622
QCARM_0002470
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QCARM_0167741
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QCARM_0339326
QCARM_0343533
QCARM_0353345
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Exhibit A to Rebuttal Expert Report of Dr. Murali Annavaram

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QCARM_3041647
QCARM_3337720
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Exhibit A to Rebuttal Expert Report of Dr. Murali Annavaram

EXPERT REPORT OF MURALI ANNAVARAM CONTAINS CONFIDENTIAL BUSINESS
INFORMATION SUBJECT TO PROTECTIVE ORDER

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Exhibit A to Rebuttal Expert Report of Dr. Murali Annavaram

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Exhibit A to Rebuttal Expert Report of Dr. Murali Annavaram

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

ARM LTD.,

       Plaintiff,

   v.

QUALCOMM INC., QUALCOMM
TECHNOLOGIES, INC. and NUVIA, INC.,

       Defendants

C.A. No. 22-1146 (MN)

REBUTTAL EXPERT REPORT OF DR. MURALI ANNAVARAM

APPENDIX B
Source Code

Appendix B contains the following documents, which have been designated as "HIGHLY CONFIDENTIAL - SOURCE CODE - ATTORNEYS' EYES ONLY" pursuant to the Protective Order in this action.

QSC2ARMVQC0000068
QSC2ARMVQC0000090
QSC2ARMVQC0000110

Pursuant to the Protective Order, a printed copy of the above-listed documents is being sent via FedEx to the offices:

Morrison & Foerster LLP
2100 L Street, NW
Suite 900
Washington, D.C., 20037
Phone: (202) 887-1500

EXHIBIT 23

Arm® Architecture Reference Manual

Armv8, for A-profile architecture

arm

ARM_01324149

Arm Architecture Reference Manual
Armv8, for A-profile architecture

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Release Information

The following releases of this document have been made.

Release history

Date	Issue	Confidentiality	Change
30 April 2013	A.a-1	Confidential-Beta Draft	Beta draft of first issue, limited circulation
12 June 2013	A.a-2	Confidential-Beta Draft	Second beta draft of first issue, limited circulation
04 September 2013	A.a	Non-Confidential Beta	Beta release
24 December 2013	A.b	Non-Confidential Beta	Second beta release
18 July 2014	A.c	Non-Confidential Beta	Third beta release
09 October 2014	A.d	Non-Confidential Beta	Fourth beta release
17 December 2014	A.e	Non-Confidential Beta	Fifth beta release
25 March 2015	A.f	Non-Confidential Beta	Sixth beta release
10 July 2015	A.g	Non-Confidential Beta	Seventh beta release
30 September 2015	A.h	Non-Confidential Beta	Eighth beta release
28 January 2016	A.i	Non-Confidential Beta	Ninth beta release
03 June 2016	A.j	Non-Confidential EAC	EAC release
30 September 2016	A.k	Non-Confidential Armv8.0 EAC	Updated EAC release
31 March 2017	B.a	Non-Confidential Armv8.1 EAC, v8.2 Beta	Initial release incorporating Armv8.1 and Armv8.2
26 September 2017	B.b	Non-Confidential Armv8.2 EAC	Initial Armv8.2 EAC release, incorporating SPE
20 December 2017	C.a	Non-Confidential Armv8.3 EAC	Initial Armv8.3 EAC release
31 October 2018	D.a	Non-Confidential Armv8.4 EAC	Initial Armv8.4 EAC release
29 April 2019	D.b	Non-Confidential Armv8.4 EAC	Updated Armv8.4 EAC release incorporating accessibility changes
05 July 2019	E.a	Non-Confidential Armv8.5 EAC	Initial Armv8.5 EAC release
20 February 2020	F.a	Non-Confidential Armv8.6 Beta	Initial Armv8.6 Beta release
31 March 2020	F.b	Non-Confidential Armv8.5 EAC, v8.6 Beta	Armv8.5 EAC release, initial Armv8.6 Beta release
17 July 2020	F.c	Non-Confidential Armv8.6 EAC	Initial Armv8.6 EAC release
22 January 2021	G.a	Non-Confidential Armv8.7 EAC	Initial Armv8.7 EAC release
22 July 2021	G.b	Non-Confidential Armv8.7 EAC	Updated Armv8.7 EAC release

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In this document, where the term Arm is used to refer to the company it means "Arm or any of its affiliates as appropriate".

────────── **Note** ──────────

• The term Arm can refer to versions of the Arm architecture, for example Armv8 refers to version 8 of the Arm architecture. The context makes it clear when the term is used in this way.

• This document describes only the Armv8-A architecture profile. For the behaviors required by the previous version of this architecture profile, ARMv7-A, see the *ARM Architecture Reference Manual, ARMv7-A and ARMv7-R edition*.

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Confidentiality Status

This document is Non-Confidential. The right to use, copy and disclose this document may be subject to license restrictions in accordance with the terms of the agreement entered into by Arm and the party that Arm delivered this document to.

Product Status

The information in this document is final, that is for a developed product.

The information in this manual is at EAC quality, which means that all features of the specification are described in the manual.

Web Address

http://www.arm.com

Limitations of this issue

This issue of the Armv8 Architecture Reference Manual contains many improvements and corrections. Validation of this document has identified the following issues that Arm will address in future issues:

• *PE state on reset to AArch64 state* on page D1-2472 and *PE state on reset into AArch32 state* on page G1-6100 require further update. Since the reset information is present in the register descriptions, this does not affect the quality status of the release.

• Appendix K14 *Arm Pseudocode Definition* requires further review and update. Since this appendix is informative, rather than being part of the architecture specification, this does not affect the quality status of this release.

- For a list of the known issues in this Manual, please refer to the Known Issues document on
  `https://developer.arm.com/documentation/102105/latest.`

- For a list of the known issues in the System register and instruction XML content, please refer to the Release Notes on
  `https://developer.arm.com/architectures/cpu-architecture/a-profile/exploration-tools.`

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Glossary

Preface

This preface introduces the *Arm Architecture Reference Manual, Armv8, for Armv8-A architecture profile*. It contains the following sections:

- *About this Manual* on page xviii.
- *Using this Manual* on page xx.
- *Conventions* on page xxvi.
- *Additional reading* on page xxviii.
- *Feedback* on page xxx.

About this Manual

This manual describes the Arm® architecture v8, Armv8. The architecture describes the operation of an Armv8-A *Processing element (PE)*, and this Manual includes descriptions of:

- The two Execution states, AArch64 and AArch32.

- The instruction sets:
  — In AArch32 state, the A32 and T32 instruction sets, that are compatible with earlier versions of the Arm architecture.
  — In AArch64 state, the A64 instruction set.

- The states that determine how a PE operates, including the current Exception level and Security state, and in AArch32 state the PE mode.

- The Exception model.

- The interprocessing model, that supports transitioning between AArch64 state and AArch32 state.

- The memory model, that defines memory ordering and memory management. This manual covers a single architecture profile, Armv8-A, that defines a *Virtual Memory System Architecture* (VMSA).

- The programmers' model, and its interfaces to System registers that control most PE and memory system features, and provide status information.

- The Advanced SIMD and floating-point instructions, that provide high-performance:
  — Single-precision, half-precision, and double-precision floating-point operations.
  — Conversions between double-precision, single-precision, and half-precision floating-point values.
  — Integer, single-precision floating-point, and half-precision floating-point vector operations in all instruction sets.
  — Double-precision floating-point vector operations in the A64 instruction set.

- The security model, that provides two Security states to support Secure applications.

- The virtualization model.

- The Debug architecture, that provides software access to debug features.

This manual gives the assembler syntax for the instructions it describes, meaning that it describes instructions in textual form. However, this Manual is not a tutorial for Arm assembler language, nor does it describe Arm assembler language, except at a very basic level. To make effective use of Arm assembler language, read the documentation supplied with the assembler being used.

This manual is organized into parts:

Part A   Provides an introduction to the Armv8-A architecture, and an overview of the AArch64 and AArch32 Execution states.

Part B   Describes the application level view of the AArch64 Execution state, meaning the view from EL0. It describes the application level view of the programmers' model and the memory model.

Part C   Describes the A64 instruction set, that is available in the AArch64 Execution state. The descriptions for each instruction also include the precise effects of each instruction when executed at EL0, described as *unprivileged* execution, including any restrictions on its use, and how the effects of the instruction differ at higher Exception levels. This information is of primary importance to authors and users of compilers, assemblers, and other programs that generate Arm machine code.

Part D   Describes the system level view of the AArch64 Execution state. It includes details of the System registers, most of which are not accessible from EL0, and the system level view of the programmers' model and the memory model. This part includes the description of self-hosted debug.

Part E   Describes the application level view of the AArch32 Execution state, meaning the view from the EL0. It describes the application level view of the programmers' model and the memory model.

———— **Note** ————
In AArch32 state, execution at EL0 is execution in User mode.

Part F   Describes the T32 and A32 instruction sets, that are available in the AArch32 Execution state. These instruction sets are backwards-compatible with earlier versions of the Arm architecture. This part describes the precise effects of each instruction when executed in User mode, described as *unprivileged* execution or execution at EL0, including any restrictions on its use, and how the effects of the instruction differ at higher Exception levels. This information is of primary importance to authors and users of compilers, assemblers, and other programs that generate Arm machine code.

———— **Note** ————
User mode is the only mode where software execution is unprivileged.

Part G   Describes the system level view of the AArch32 Execution state, that is generally compatible with earlier versions of the Arm architecture. This part includes details of the System registers, most of which are not accessible from EL0, and the instruction interface to those registers. It also describes the system level view of the programmers' model and the memory model.

Part H   Describes the Debug architecture for external debug. This provides configuration, breakpoint and watchpoint support, and a *Debug Communications Channel* (DCC) to a debug host.

Part I   Describes additional features of the architecture that are not closely coupled to a *processing element* (PE), and therefore are accessed through memory-mapped interfaces. Some of these features are OPTIONAL.

Part J   Provides pseudocode that describes various features of the Armv8 architecture.

Part K, Appendixes

Provide additional information. Some appendixes give information that is not part of the Armv8 architectural requirements. The cover page of each appendix indicates its status.

Glossary   Defines terms used in this document that have a specialized meaning.

———— **Note** ————
Terms that are generally well understood in the microelectronics industry are not included in the Glossary.

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Using this Manual

The information in this Manual is organized into parts, as described in this section.

Part A, Introduction and Architecture Overview

Part A gives an overview of the Armv8-A architecture profile, including its relationship to the other Arm PE architectures. It introduces the terminology used to describe the architecture, and gives an overview of the Executions states, AArch64 and AArch32. It contains the following chapter:

Chapter A1 *Introduction to the Armv8 Architecture*

> Read this for an introduction to the Armv8 architecture.

Chapter A2 *Armv8-A Architecture Extensions*

> Read this for an introduction to the Armv8 architecture extensions.

Part B, The AArch64 Application Level Architecture

Part B describes the AArch64 state application level view of the architecture. It contains the following chapters:

Chapter B1 *The AArch64 Application Level Programmers' Model*

> Read this for an application level description of the programmers' model for software executing in AArch64 state. It describes execution at EL0 when EL0 is using AArch64 state.

Chapter B2 *The AArch64 Application Level Memory Model*

> Read this for an application level description of the memory model for software executing in AArch64 state. It describes the memory model for execution in EL0 when EL0 is using AArch64 state. It includes information about Arm memory types, attributes, and memory access controls.

Part C, The A64 Instruction Set

Part C describes the A64 instruction set, that is used in AArch64 state. It contains the following chapters:

Chapter C1 *The A64 Instruction Set*

> Read this for a description of the A64 instruction set and common instruction operation details.

Chapter C2 *About the A64 Instruction Descriptions*

> Read this to understand the format of the A64 instruction descriptions.

Chapter C3 *A64 Instruction Set Overview*

> Read this for an overview of the individual A64 instructions, that are divided into five functional groups.

Chapter C4 *A64 Instruction Set Encoding*

> Read this for a description of the A64 instruction set encoding.

Chapter C5 *The A64 System Instruction Class*

> Read this for a description of the AArch64 System instructions and register descriptions, and the System instruction class encoding space.

Chapter C6 *A64 Base Instruction Descriptions*

> Read this for information on key aspects of the A64 base instructions and for descriptions of the individual instructions, which are listed in alphabetical order.

Chapter C7 *A64 Advanced SIMD and Floating-point Instruction Descriptions*

> Read this for information on key aspects of the A64 Advanced SIMD and floating-point instructions and for descriptions of the individual instructions, which are listed in alphabetical order.

Part D, The AArch64 System Level Architecture

Part D describes the AArch64 state system level view of the architecture. It contains the following chapters:

Chapter D1 *The AArch64 System Level Programmers' Model*

Read this for a description of the AArch64 state system level view of the programmers' model.

Chapter D2 *AArch64 Self-hosted Debug*

Read this for an introduction to, and a description of, self-hosted debug in AArch64 state.

Chapter D3 *AArch64 Self-hosted Trace*

Read this for an introduction to, and a description of, self-hosted trace in AArch64 state.

Chapter D4 *The AArch64 System Level Memory Model*

Read this for a description of the AArch64 state system level view of the general features of the memory system.

Chapter D5 *The AArch64 Virtual Memory System Architecture*

Read this for a system level view of the AArch64 Virtual Memory System Architecture (VMSA), the memory system architecture of an Armv8 implementation executing in AArch64 state.

Chapter D7 *The Performance Monitors Extension*

Read this for a description of an implementation of the Arm Performance Monitors, an optional non-invasive debug component.

Chapter D8 *The Activity Monitors Extension*

Read this for a description of an implementation of the Arm Activity Monitors, an optional non-invasive component.

Chapter D9 *The Statistical Profiling Extension*

Read this for a description of an implementation of the Statistical Profiling Extension, an optional AArch64 state non-invasive debug component.

Chapter D10 *Statistical Profiling Extension Sample Record Specification*

Read this for a description the sample records generated by the Statistical Profiling Extension.

Chapter D11 *The Generic Timer in AArch64 state*

Read this for a description of the AArch64 view of an implementation of the Arm Generic Timer.

Chapter D12 *AArch64 System Register Encoding*

Read this for a description of the encoding of the AArch64 System registers, and the other uses of the AArch64 System registers encoding space.

Chapter D13 *AArch64 System Register Descriptions*

Read this for an introduction to, and description of, each of the AArch64 System registers.

Part E, The AArch32 Application Level Architecture

Part E describes the AArch32 state application level view of the architecture. It contains the following chapters:

Chapter E1 *The AArch32 Application Level Programmers' Model*

Read this for an application level description of the programmers' model for software executing in AArch32 state. It describes execution at EL0 when EL0 is using AArch32 state.

Chapter E2 *The AArch32 Application Level Memory Model*

Read this for an application level description of the memory model for software executing in AArch32 state. It describes the memory model for execution in EL0 when EL0 is using AArch32 state. It includes information about Arm memory types, attributes, and memory access controls.

Part F, The AArch32 Instruction Sets

Part F describes the T32 and A32 instruction sets, that are used in AArch32 state. It contains the following chapters:

Chapter F1 *About the T32 and A32 Instruction Descriptions*

Read this to understand the format of the T32 and A32 instruction descriptions.

Chapter F2 *The AArch32 Instruction Sets Overview*

Read this for an overview of the T32 and A32 instruction sets.

Chapter F3 *T32 Instruction Set Encoding*

Read this for a description of the T32 instruction set encoding. This includes the T32 encoding of the Advanced SIMD and floating-point instructions.

Chapter F4 *A32 Instruction Set Encoding*

Read this for a description of the A32 instruction set encoding. This includes the A32 encoding of the Advanced SIMD and floating-point instructions.

Chapter F5 *T32 and A32 Base Instruction Set Instruction Descriptions*

Read this for a description of each of the T32 and A32 base instructions.

Chapter F6 *T32 and A32 Advanced SIMD and Floating-point Instruction Descriptions*

Read this for a description of each of the T32 and A32 Advanced SIMD and floating-point instructions.

Part G, The AArch32 System Level Architecture

Part G describes the AArch32 state system level view of the architecture. It contains the following chapters:

Chapter G1 *The AArch32 System Level Programmers' Model*

Read this for a description of the AArch32 state system level view of the programmers' model for execution in an Exception level that is using AArch32.

Chapter G2 *AArch32 Self-hosted Debug*

Read this for an introduction to, and a description of, self-hosted debug in AArch64 state.

Chapter G3 *AArch32 Self-hosted Trace*

Read this for an introduction to, and a description of, self-hosted trace in AArch64 state.

Chapter G4 *The AArch32 System Level Memory Model*

Read this for a system level view of the general features of the memory system.

Chapter G5 *The AArch32 Virtual Memory System Architecture*

Read this for a description of the AArch32 Virtual Memory System Architecture (VMSA).

Chapter G6 *The Generic Timer in AArch32 state*

Read this for a description of the AArch32 view of an implementation of the Arm Generic Timer.

Chapter G7 *AArch32 System register Encoding*

Read this for a description of the encoding of the AArch32 System registers, including the System instructions that are part of the AArch32 System registers encoding space.

Chapter G8 *AArch32 System Register Descriptions*

Read this for a description of each of the AArch32 System registers.

Part H, External Debug

Part H describes the architecture for external debug. It contains the following chapters:

Chapter H1 *About External Debug*

> Read this for an introduction to external debug, and a definition of the scope of this part of the manual.

Chapter H2 *Debug State*

> Read this for a description of Debug state, which the PE might enter as the result of a Halting debug event.

Chapter H3 *Halting Debug Events*

> Read this for a description of the external debug events referred to as Halting debug events.

Chapter H4 *The Debug Communication Channel and Instruction Transfer Register*

> Read this for a description of the communication between a debugger and the PE debug logic using the Debug Communications Channel and the Instruction Transfer register.

Chapter H5 *The Embedded Cross-Trigger Interface*

> Read this for a description of the embedded cross-trigger interface.

Chapter H6 *Debug Reset and Powerdown Support*

> Read this for a description of reset and powerdown support in the Debug architecture.

Chapter H7 *The PC Sample-based Profiling Extension*

> Read this for a description of the PC Sample-based Profiling Extension that is an OPTIONAL extension to an Armv8 implementation.

Chapter H8 *About the External Debug Registers*

> Read this for some additional information about the external debug registers.

Chapter H9 *External Debug Register Descriptions*

> Read this for a description of each external debug register.

Part I, Memory-mapped Components of the Armv8 Architecture

Part I describes the memory-mapped components in the architecture. It contains the following chapters:

Chapter I1 *Requirements for Memory-mapped Components*

> Read this for descriptions of some general requirements for memory-mapped components within a system that complies with the Armv8 Architecture.

Chapter I2 *System Level Implementation of the Generic Timer*

> Read this for a definition of a system level implementation of the Generic Timer.

Chapter I3 *Recommended External Interface to the Performance Monitors*

> Read this for a description of the recommended memory-mapped and external debug interfaces to the Performance Monitors.

Chapter I4 *Recommended External Interface to the Activity Monitors*

> Read this for a description of the recommended memory-mapped interface to the Activity Monitors.

Chapter I5 *External System Control Register Descriptions*

> Read this for a description of each memory-mapped system control register.

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Part J, Architectural Pseudocode

Part J contains pseudocode that describes various features of the Arm architecture. It contains the following chapter:

Chapter J1 *Armv8 Pseudocode*

Read this for the pseudocode definitions that describe various features of the Armv8 architecture, for operation in AArch64 state and in AArch32 state.

Part K, Appendixes

This manual contains the following appendixes:

Appendix K1 *Architectural Constraints on UNPREDICTABLE Behaviors*

Read this for a description of the architecturally-required constraints on UNPREDICTABLE behaviors in the Armv8 architecture, including AArch32 behaviors that were UNPREDICTABLE in previous versions of the architecture.

Appendix K2 *Recommended External Debug Interface*

Read this for a description of the recommended external debug interface.

——— **Note** ———

This description is not part of the Arm architecture specification. It is included here as supplementary information, for the convenience of developers and users who might require this information.

Appendix K3 *Recommendations for Performance Monitors Event Numbers for IMPLEMENTATION DEFINED Events*

Read this for a description of Arm recommendations for the use of the IMPLEMENTATION DEFINED event numbers.

——— **Note** ———

This description is not part of the Arm architecture specification. It is included here as supplementary information, for the convenience of developers and users who might require this information.

Appendix K4 *Recommendations for Reporting Memory Attributes on an Interconnect*

Read this for the Arm recommendations about how the architectural memory attributes are reported on an interconnect.

Appendix K5 *Additional Information for Implementations of the Generic Timer*

Read this for additional information about implementations of the Arm Generic Timer. This information does not form part of the architectural definition of the Generic Timer.

Appendix K6 *Legacy Instruction Syntax for AArch32 Instruction Sets*

Read this for information about the pre-UAL syntax of the AArch32 instruction sets, which can still be valid for the A32 instruction set.

Appendix K7 *Address Translation Examples*

Read this for examples of translation table lookups using the translation regimes described in Chapter D5 *The AArch64 Virtual Memory System Architecture* and Chapter G5 *The AArch32 Virtual Memory System Architecture*.

Appendix K8 *Example OS Save and Restore Sequences*

Read this for software examples that perform the OS Save and Restore sequences for an Armv8 debug implementation.

———— Note ————

Chapter H6 *Debug Reset and Powerdown Support* describes the OS Save and Restore mechanism.

————————————————

Appendix K9 *Recommended Upload and Download Processes for External Debug*

Read this for information about implementing and using the Arm architecture.

———— Note ————

This description is not part of the Arm architecture specification. It is included here as supplementary information, for the convenience of developers and users who might require this information.

————————————————

Appendix K10 *Software Usage Examples*

Read this for software examples that help understanding of some aspects of the Arm architecture.

———— Note ————

This description is not part of the Arm architecture specification. It is included here as supplementary information, for the convenience of developers and users who might require this information.

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Appendix K11 *Barrier Litmus Tests*

Read this for examples of the use of barrier instructions provided by the Armv8 architecture.

———— Note ————

This description is not part of the Arm architecture specification. It is included here as supplementary information, for the convenience of developers and users who might require this information.

————————————————

Appendix K14 *Arm Pseudocode Definition*

Read this for definitions of the AArch32 pseudocode.

Appendix K15 *Registers Index*

Read this for an alphabetic and functional index of AArch32 and AArch64 registers, and memory-mapped registers.

Glossary

Defines terms used in this document that have a specialized meaning.

———— Note ————

Terms that are generally well understood in the microelectronics industry are not included in the Glossary.

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Conventions

The following sections describe conventions that this book can use:

- *Typographic conventions* on page xxvi.
- *Signals* on page xxvii.
- *Numbers* on page xxvii.
- *Pseudocode descriptions* on page xxvii.
- *Assembler syntax descriptions* on page xxvii.

Typographic conventions

The typographical conventions are:

italic
Introduces special terminology, and denotes citations.

bold
Denotes signal names, and is used for terms in descriptive lists, where appropriate.

monospace
Used for assembler syntax descriptions, pseudocode, and source code examples.

Also used in the main text for instruction mnemonics and for references to other items appearing in assembler syntax descriptions, pseudocode, and source code examples.

SMALL CAPITALS
Used in body text for a few terms that have specific technical meanings, and are defined in the *Glossary*.

Colored text
Indicates a link. This can be:

- A URL, for example https://developer.arm.com.
- A cross-reference, that includes the page number of the referenced information if it is not on the current page, for example, *Assembler syntax descriptions* on page xxvii.
- A link, to a chapter or appendix, or to a glossary entry, or to the section of the document that defines the colored term, for example *Simple sequential execution* or SCTLR.

{ and }
Braces, { and }, have two distinct uses:

Optional items
In syntax descriptions braces enclose optional items. In the following example they indicate that the <shift> parameter is optional:

```
ADD <Wd|WSP>, <Wn|WSP>, #<imm>{, <shift>}
```

Similarly they can be used in generalized field descriptions, for example TCR_ELx.{I}PS refers to a field in the TCR_ELx registers that is called either IPS or PS.

Sets of items
Braces can be used to enclose sets. For example, HCR_EL2.{E2H, TGE} refers to a set of two register fields, HCR_EL2.E2H and HCR_EL2.TGE

Notes
Notes are formatted as:

——— **Note** ———
This is a Note.

In this Manual, Notes are used only to provide additional information, usually to help understanding of the text. While a Note may repeat architectural information given elsewhere in the Manual, a Note never provides any part of the definition of the architecture.

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Signals

In general this specification does not define hardware signals, but it does include some signal examples and recommendations. The signal conventions are:

Signal level   The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n   At the start or end of a signal name denotes an active-LOW signal.

Numbers

Numbers are normally written in decimal. Binary numbers are preceded by `0b`, and hexadecimal numbers by `0x`. In both cases, the prefix and the associated value are written in a `monospace` font, for example `0xFFFF0000`. To improve readability, long numbers can be written with an underscore separator between every four characters, for example `0xFFFF_0000_0000_0000`. Ignore any underscores when interpreting the value of a number.

Pseudocode descriptions

This manual uses a form of pseudocode to provide precise descriptions of the specified functionality. This pseudocode is written in `monospace` font, and is described in Appendix K14 *Arm Pseudocode Definition*.

Assembler syntax descriptions

This manual contains numerous syntax descriptions for assembler instructions and for components of assembler instructions. These are shown in a `monospace` font, and use the conventions described in *Structure of the A64 assembler language* on page C1-195, and Appendix K14 *Arm Pseudocode Definition*.

Additional reading

This section lists relevant publications from Arm and third parties.

See Arm Developer, `https://developer.arm.com`, for access to Arm documentation.

Arm publications

- *ARM® AMBA® 4 ATB Protocol Specification, ATBv1.0 and ATBv1.1*, (ARM IHI 0032B).

- *ARM® Architecture Reference Manual, ARMv7-A and ARMv7-R edition* (ARM DDI 0406).

- *ARM® Architecture Reference Manual Supplement, ARMv8, for the ARMv8-R AArch32 architecture profile* (ARM DDI 0568).

- *ARM® Debug Interface Architecture Specification, ADIv6.0* (ARM IHI 0074).

- *ARM® Debug Interface Architecture Specification, ADIv5.0 to ADIv5.2* (ARM IHI 0031).

- *ARM® Embedded Trace Macrocell Architecture Specification, ETMv4* (ARM IHI 0064).

- *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0* (ARM IHI 0069).

- *ARM® CoreSight™ SoC Technical Reference Manual* (ARM DDI 0480).

- *ARM® CoreSight™ Architecture Specification* (ARM IHI 0029).

- *ARM® Procedure Call Standard for the ARM 64-bit Architecture* (ARM IHI 0055).

- *Arm® Reliability, Availability, and Serviceability (RAS) Specification, Armv8, for the Armv8-A architecture profile* (ARM DDI 0587).

- *Arm® Architecture Reference Manual Supplement, The Scalable Vector Extension (SVE), for Armv8-A* (ARM DDI 0584).

- *Arm® Architecture Reference Manual Supplement, Memory System Resource Partitioning and Monitoring (MPAM), for A-Profile Architecture* (ARM DDI 0598).

Other publications

The following publications are referred to in this Manual, or provide more information:

- *Announcing the Advanced Encryption Standard (AES)*, Federal Information Processing Standards Publication 197, November 2001.

- IEEE Std 754-2008, *IEEE Standard for Floating-point Arithmetic*, August 2008.

- IEEE Std 754-1985, *IEEE Standard for Floating-point Arithmetic*, March 1985.

- *Secure Hash Standard (SHA)*, Federal Information Processing Standards Publication 180-2, August 2002.

- *The Galois/Counter Mode of Operation*, McGraw, D. and Viega, J., Submission to NIST Modes of Operation Process, January 2004.

- *Memory Consistency Models for Shared Memory-Multiprocessors*, Gharachorloo, Kourosh, 1995, Stanford University Technical Report CSL-TR-95-685.

- *Standard Manufacturer's Identification Code, JEP106*, JEDEC Solid State Technology Association.

- *SM3 Cryptographic Hash Algorithm*, China Internet Network Information Center (CNNIC).

- *SM4 Block Cipher Algorithm*, China Internet Network Information Center (CNNIC).

- *The QARMA Block Cipher Family*, Roberto Avanzi, Qualcomm Product Security Initiative.

Available from `https://eprint.iacr.org/2016/444.`

Feedback

Arm welcomes feedback on its documentation.

Feedback on this Manual

If you have comments on the content of this Manual, send email to errata@arm.com. Give:
- The title, *Arm® Architecture Reference Manual, Armv8, for Armv8-A architecture profile.*
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Previous issues of this document included terms that can be offensive. We have replaced these terms. If you find offensive terms in this document, please contact terms@arm.com.

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